Honeywell

HONEYWELL
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8708671 Rev 7-88

A.1.1 Matrix Processor Architecture

The Honeywell Matrix Processor functional element (MPFE) is a loosely coupled, coarse-grain architecture that expands as a "circuit hypercube" using our hypercube interconnect network (HIN). Each processor has substantial capacity and memory that is not shared.

Our MP is modular. It can be a single MPC extended with from one to eight FPAs on the local expansion bus (E-bus) as shown in Exhibit A-2. It can also be expanded on the MPFE HIN with additional MPCs with a total of up to 64 MPCs and up to 512 FPAs. Thus, a single MPFE can provide up to 337 GFLOPS.

The hypercube uses a message-passing network between MPs (one MP at each hypercube hardware node). The hypercube interconnect is an optimal topology that minimizes the number of interconnects in a distributed architecture, while minimizing the number of intermediate links and thus minimizing latency for message traffic between hypercube nodes. Within each MP node there are medium-grain floating-point processors and control subsystems that share a 4-GB address space.

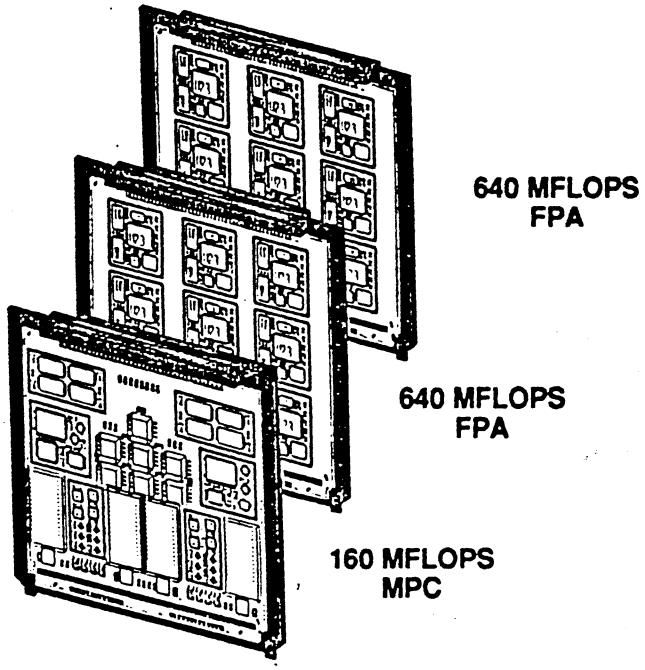

Exhibit A-1. Matrix Processor SEM E Module Types

Our Matrix Processor architecture is based on only two new SEM E module types, yet offers 1.44 GFLOPS as an expandable architecture.

A.1.3 Hypercube Interconnect Network (HIN) Architecture Description

The generic hypercube architecture is shown in Exhibit A-5. Each node in the hypercube is an MPC with its attached FPAs. The hypercube architecture has been proven in commercially successful supercomputers such as Intel Scientific Computers' iPSC/2™ (more than 150 sold), Thinking Machines' Connection Machine, and others. The MPC hypercube interconnection architecture is a low-development-risk, high-performance, militarized version of commercial hypercube implementations. This well-proven supercomputer architecture offers universal interconnectivity among the MPs with a minimal number of serial interconnect links. For example, each MPC in a 32-node hypercube uses five bidirectional serial-40 Mbps links, one to each of its nearest neighbor nodes in the hypercube. Our 32-node HIN provides 320 MB per second of aggregate interconnect bandwidth. To achieve the same performance, a 32-bit-wide parallel bus would have to be clocked at 80 MHz and a serial ring would have to clock at more than 2.5 GHz. We have avoided these network approaches because their speed requirements exceed design limitations. Messages are automatically routed through intermediate nodes as necessary in order to reach more distant nodes. A straightforward routing algorithm is implemented in silicon on each MPC. This reduces the MPC processor load to only those messages for which it is the ultimate destination. The hypercube internode connectivity is managed by the MPC operating system. It provides a message-passing communication service to application processes running in the MPC, which removes the programmer's need to understand or manage the details of the hypercube architecture.

Although far fewer links are used than a fully interconnected network would require, redundant paths are available between nodes. Applying exclusive OR to the binary source and destination node addresses forms a unique routing vector. Each position in the vector is a dimension in the cube (it is also an interconnect network port number). Each "one" in the routing vector represents a move or hop along that dimension. Because the dimensions are orthogonal the sequence of moves can be taken in any order. The different sequences possible generate the redundant paths. Our routing method takes advantage of this available redundancy to provide maximum communications bandwidth and to route around failed nodes. Hypercubes for military use have been limited by the need to populate them in powers of two to make the typical routing algorithms work. Doubling a 16-node configuration to 32 nodes just to gain a few additional nodes' worth of processing may be too costly for many applications. Our independent research and development (IR&D) efforts have resulted in a routing method based on storing at each node at system initialization time the actual configuration of nodes (not limited to a power of two). We can configure the hypercube as 1, 2, or in multiples of four nodes and still not experience failures of communications among working nodes when a node fails. This provides graceful degradation of MP the basis for performance.

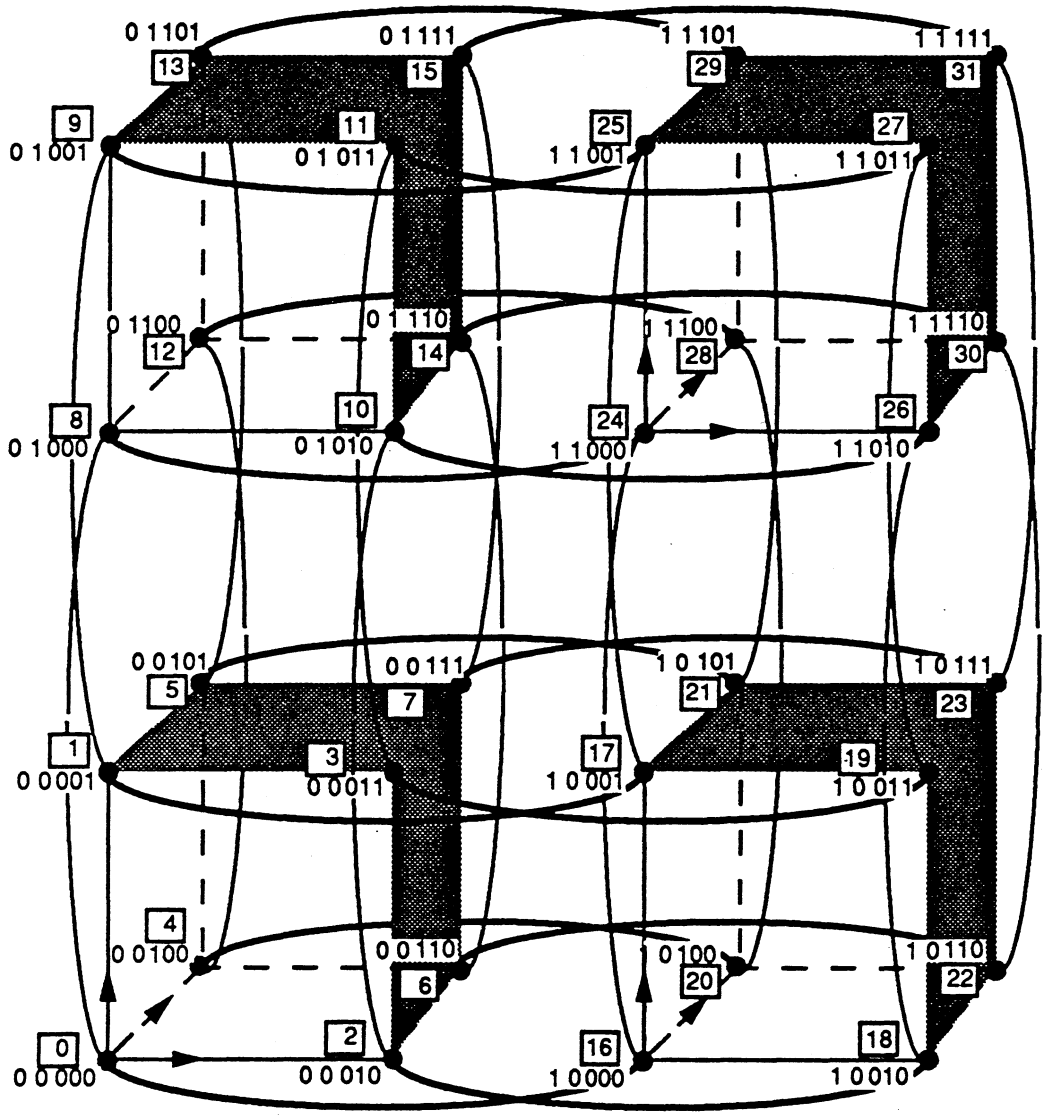

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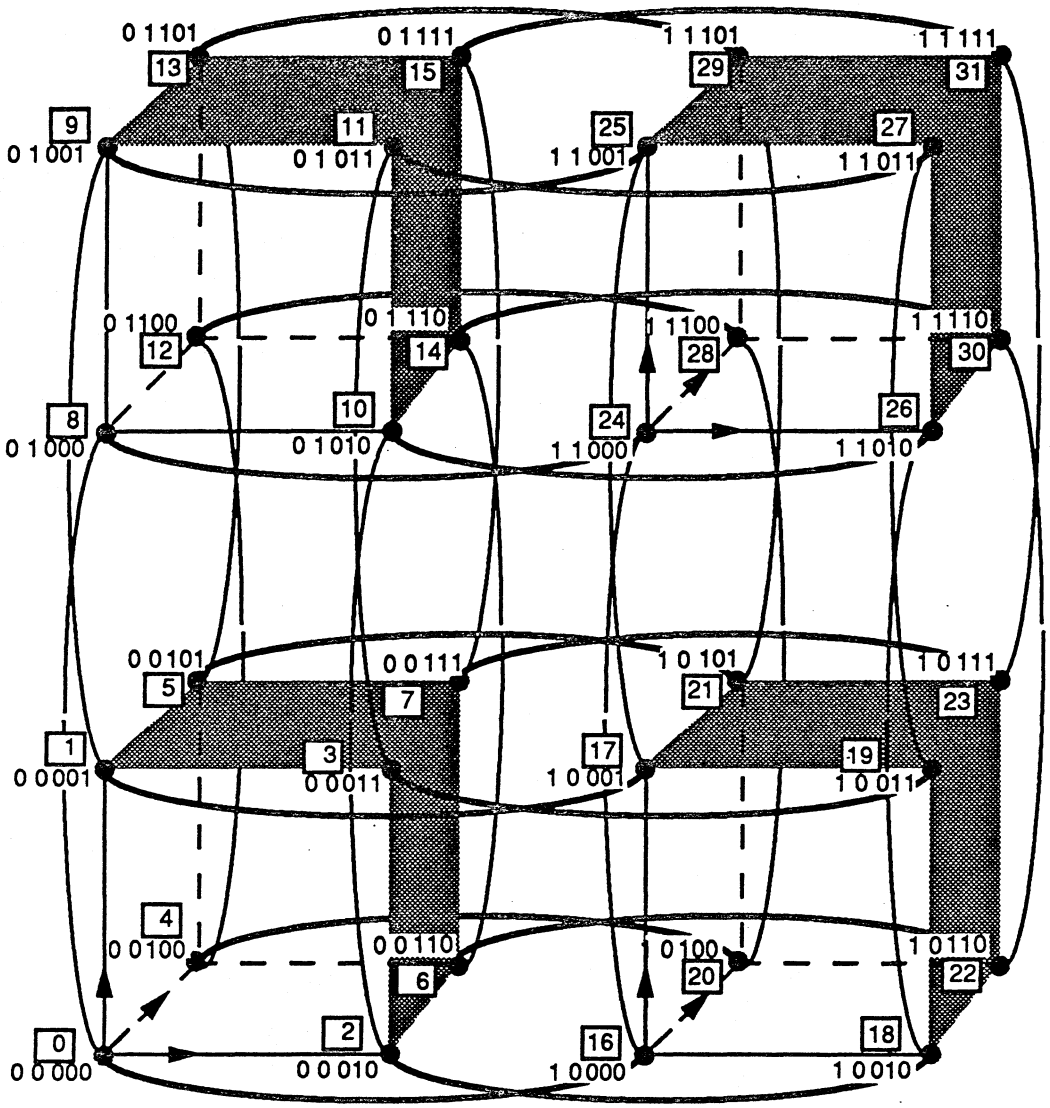
Exhibit A-5. Hypercube Interconnect Network Architecture

Our hypercube interconnect network (HIN) offers universal interconnectivity in configurations up to 64 Matrix Processors and is the most efficient expandable network known. A 32-MP configuration is shown here.



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** TX CONFIRMATION REPORT ** AS OF SEP 24 '90 16:06 PAGE.01

HONEYWELL MSD MK 50

	DATE	TIME	TO/FROM	MODE	MIN/SEC	PGS	STATUS
01	9/24	15:59	8-7032736608	EC--SR	07"37	13/ 00	INC

PRODUCT SPECIFICATIONS

Processors	4096	8192	16,384	32,768	65,536
Memory	128 Mbytes	256 Mbytes	512 Mbytes	1 Gbyte	2 Gbytes
Performance (Processor)					
32-bit integer add	150 Mips	300 Mips	600 Mips	1200 Mips	2500 Mips
8-bit byte add	250 Mips	500 Mips	1000 Mips	2000 Mips	4000 Mips
4K x 4K Matrix Multiply					
32-bit IEEE floating point	310 MFlops (2K x 2K)	625 MFlops	1250 MFlops	2500 MFlops	5000 MFlops
64-bit IEEE floating point	–	–	625 MFlops	1250 MFlops	2500 MFlops
Dot Product					
32-bit IEEE floating point	625 MFlops	1250 MFlops	2500 MFlops	5000 MFlops	10,000 MFlops
64-bit IEEE floating point	–	–	1250 MFlops	2500 MFlops	5000 MFlops
Performance (Example Applications)					
Poisson's Equation (32-bit)	230 MFlops	475 MFlops	950 MFlops	1900 MFlops	3800 MFlops
Wave Equation (32-bit)	120 MFlops	250 MFlops	500 MFlops	1000 MFlops	2000 MFlops
Languages	*Lisp, C*	*Lisp, C*	*Lisp, C*	*Lisp, C*	*Lisp, C*
	Fortran 8X	Fortran 8X	Fortran 8X	Fortran 8X	Fortran 8X
Front End Systems	Sun 4, VAX 6300	Sun 4, VAX 6300	Sun 4, VAX 6300	Sun 4, VAX 6300	Sun 4, VAX 6300
	Symbolics	Symbolics	Symbolics	Symbolics	Symbolics
Input/Output Channels					
Number of Channels	2	2	4	8	8
Capacity per channel	50 Mbytes/sec	50 Mbytes/sec	50 Mbytes/sec	50 Mbytes/sec	50 Mbytes/sec
Maximum Transfer Rate	50 Mbytes/sec	50 Mbytes/sec	100 Mbytes/sec	200 Mbytes/sec	400 Mbytes/sec
Environmental Requirements					
Power	30 amp 1-phase	30 amp 1-phase	30 amp 3-phase	30 amp 3-phase	30 amp 3-phase
Voltage	200-240	200-240	110/208Y	110/208Y	110/208Y
Hertz	50/60	50/60	50/60	50/60	50/60
Power Dissipation	3.5 KVA	3.5 KVA	7 KVA	14 KVA	28 KVA
Size	26" x 26" x 43"	26" x 26" x 43"	56" x 56" x 62"	56" x 56" x 62"	56" x 56" x 62"
Weight	375 lbs.	375 lbs.	1200 lbs.	1800 lbs.	3000 lbs.
Operating Temperature	70°F ± 5°F	70°F ± 5°F	70°F ± 5°F	70°F ± 5°F	70°F ± 5°F
Relative Humidity	50% ± 10%	50% ± 10%	50% ± 10%	50% ± 10%	50% ± 10%

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