EK-DL11W-MM-PRE

P R E L I M I N A R Y

DL11-W

SERIAL LINE UNIT/REAL-TIME CLOCK OPTION

MAINTENANCE MANUAL

Written by PDP-11 Engineering

Printed in U.S.A.

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The DL11-W Serial Line Unit/Real-Time Clock Option provides two distinct functions. First, the DL11-W is a character-buffered communications interface designed to assemble or disassemble the serial information required by a communications device for parallel transfer to or from the PDP-11 Unibus. Second, the DL11-W is a line frequency clock which can provide timed interrupts, allowing a program to measure passage of time. The DL11-W consists of a single integrated circuit quad board containing two independent communications units (receiver and transmitter) capable of simultaneous two-way communication and an independent line frequency real-time clock.

The DL11-W interface provides the logic and buffer registers necessary for program-controlled transfer of data between a PDP-11 system requiring parallel data and an external device requiring serial data. The interface also includes status and control bits that may be controlled by the program, the interface, or an external device for command, monitoring, and interrupt functions.

The DL11-W interface provides the flexibility needed to handle a variety of terminals. For example, the user can use a DL11-W as a Teletype(R) control or, in conjunction with another serial line interface, it can be used as a communications link between two processor systems. The DL11-W provides the user with a choice of line speeds (baud rates), character size, stop-code length, parity selection, and status indications.

The DL11-W can replace DL11-A, DL11-B, DL11-C, and DL11-D modules in most applications. However, the DL11-E is still required for use with communications data sets such as Bell Model 103 or 202. All of the features of the DL11-A through DL11-D modules are combined on the

(R) Teletype is a registered trademark of Teletype Corporation.

DL11-W and are switch selectable to allow for ease of interchangeability.

1.2 SCOPE

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the DL11-W SLU/RTC option. The level of discussion assumes that the reader is familiar with basic digital computer theory.

The manual is divided into five major chapters: Introduction, General Description, Installation and Configuration, Programming, and Theory of Operation. A complete set of engineering drawings is provided with each DL11-W interface and is bound in a separate volume entitled DL11-W SLU/RTC Option Engineering Drawings.

Although control signals and data are transferred between the interface and the Unibus, and between the interface and the communications device, this manual is limited to coverage of the interface itself.

Table 1-1 lists related PDP-11 system documents that are applicable to the DL11-W SLU/RTC Option. Table 1-2 lists documents applicable to communications devices that may be used with the interface. Note that this latter table lists only representative manuals, and is not intended to be an all-inclusive list.

1.3 MAINTENANCE

The basic maintenance philosophy of the DL11-W SLU/RTC Option is to present the user with the information necessary to understand normal system operation. The user can utilize this information when analyzing trouble symptoms to determine necessary corrective action. It is beyond the scope of this manual to present detailed troubleshooting information.

Table 1-1

Applicable PDP-11 Documents

Title	Number	Description
Unibus Interface Manual, Second Edition	DEC-11-HIABB-D	Provides detailed theory, flow, and logic descriptions of the Unibus and external device logic;
*PDP-11/20 System (7-volume series)	DEC-11-HR1B-D through DEC-11-HR7B-D	Provides detailed theory of operation, flow, logic diagrams, operation, installation, and maintenance for components of the PDP-11 system including processor, memory, console, and power supply.
PDP-11 Processor Handbook	DEC, 1972	A two-part general handbook. The first part discusses system architecture, addressing modes, the instruction set, and programming techniques. The second part is devoted to a discussion of software.
PDP-11 Peripherals and Interfacing Handbook	DEC, 1972	A two-part handbook. The first part is devoted to a discussion of the various peripherals used with PDP-11 systems. The second part provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and

* Applicable PDP-11/05, 11/15, 11/04, 11/34, and 11/45 manuals provide coverage on other PDP-11 sytems.

		examples of typical interfaces.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming and the floating-point and math package.

Table 1-2

Applicable Device Documents

Title	Number	Description
Automatic Send-Receive Sets, Manual	Bulletin 273B (two volumes) Teletype Corp.	Describes operation and maintenance of the Model 33 ASR Teletype unit used as an input/output device.
Model 3 Page Printer Set, Parts	Bulletin 1184B Teletype Corp.	Contains an illustrated parts breakdown to serve as a guide for disassembly, reassembly, and parts ordering for the Model 33 ASR Teletype unit.

NOTE

Comparable manuals exist for other available Teletypes such as the Model 28, Model 35, and Model 37.

VT05 Alphanumeric Display Terminal	DEC-00-H4AB-D	Describes purpose and operation of the VT05 Display used as an input/output device.
VT05 Alphanumeric Display Terminal, Maintenance Manuals,	DEC-00-H4BA-D	Provides detailed theory of operation and maintenance procedures for the VT05 Display.
VT06 Maintenance Manual	Datapoint Corp.	Provides detailed theory of operation and maintenance data for the VT06 Data Display Terminal.
LA36 DECWRITER II Users Manual	EK-LA36-OP-001	Describes purpose and and operation of LA36 Decwriter used as an input/output device.

1.4 ENGINEERING DRAWINGS

A complete set of engineering and circuit schematics is provided in a companion volume to this manual entitled DL11-W SLU/RTC Option, Engineering Drawings. The general logic symbols used on these drawings are described in the DEC Logic Handbook, 1971. Specific symbols and conventions are also included in certain PDP-11 system manuals. The following paragraphs describe the signal nomenclative convention used on the drawing set.

Signal names in the DL11-W print set are in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block (DL-1, DL-2, DL-3, etc).

SIGNAL NAME is the name proper of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3V; L means ground.

As an example, the signal:

DL-1 RCVR DONE H

originates on sheet 1 of the M7856 module drawing and is read, "when RCVR DONE is true, this signal is at +3V".

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exists. Each Unibus signal name is prefixed with the word BUS.

CHAPTER 2

GENERAL DESCRIPTION

2.1 INTRODUCTION

The DL11-W SLU/RTC option is a character-buffered communications interface designed to translate serial bit stream data to parallel character data and to provide timed interrupts to allow program time measurements. The DL11-W interface contains two independent communications units (receiver and transmitter) capable of 2-way communication.

Switch selections on the DL11-W interface provide the flexibility needed to handle a variety of terminals. For example, the user can set up switches such that the DL11-W can interface to a teletype or, by resetting switches, to a high speed CRT terminal. The user has a choice of speeds, character size, stop-code length, parity, error detection, and 20ma current loop modes.

This chapter is divided into five major portions: switch selections, data format, functional description, physical description, and specifications.

2.2 SWITCH SELECTIONS

The DL11-W may be modified by the setup of switches to allow it to directly replace a DL11-A, -B, -C, or -D module in most applications. Table 2-1 includes a list of these selections with a brief description.

Switches used on the DL11-W are clip-mounted packs containing either eight or ten individual slide or toggle switches. There are five packs mounted on the M7856 module. They are labeled on the board as S1 through S5. The switch packs (See Figure 2-1) are labeled such that each switch is numbered (1 through 8 or 10). Each pack is also labeled showing the on and off positions. The convention used to specify a particular switch is this:

SX=Y

where X indicates the switch pack number and Y indicates the particular switch on that switch pack.

For example S2=9 indicates switch number 9 on switch pack S2.

To be supplied.

Figure 2-1

Table 2-1

DL11-W Compatability Switches

SELECTABLE	SWITCH(S)	DESCRIPTION
Break Bit	S4-1	Enabled in the ON position. Should be disabled (switch OFF) if replacing a DL11-A, or DL11-B should be enabled (switch ON) if replacing a DL11-C or DL11-D.
Error Bits	S4-7	Error bit reporting is enabled in the ON position. Should be disabled if replacing DL11-A or DL11-B, and should be enabled if replacing DL11-C or DL11-D.
Real-Time Clock	S5-9 S5-10	Enabled if S5-10 is in ON position and S5-9 is in OFF position. To disable S5-10 must be OFF and S5-9 must be ON. Should be disabled if replacing DL11-A, -B, -C, or -D module with DL11-W.

Table 2-2 lists the baud rates available on the DL11-W. Completely independent split-speed operation is provided by individually selecting the receiver and transmitter baud rates. Care should be taken that both transmit and receive speeds are correct when replacing a DL11-A, -B, etc. module.

Table 2-2

Baud Rate Selection

Baud Rates	Transmitter			Receiver		
	S4-10	S3-1	S3-4	S3-2	S3-3	S3-5
110	ON	ON	ON	OFF	OFF	OFF
150	OFF	ON	ON	ON	OFF	OFF
300	ON	OFF	OFF	OFF	ON	ON
600	ON	OFF	ON	OFF	ON	OFF
1200	ON	ON	OFF	OFF	OFF	ON
2400	OFF	OFF	OFF	ON	ON	ON
4800	OFF	OFF	ON	ON	ON	OFF
9600	OFF	ON	OFF	ON	OFF	ON

Two switch selectable modes of operation are available for the 20ma current loops. These two modes of operation allow greater versatility in using the 20ma current loop interfaces.

In Active mode, the DL11-W is the source for the 20ma of current whereas in Passive mode, the external device must provide the current. An example of the application of these modes would be to connect two processing systems together using two DL11-Ws via the 20ma current loops. One DL11-W should be the active device, the other DL11-W passive. Table 2-3 shows the switch settings to select the mode of operation of the 20ma current loops. Normal configuration is in the Active mode.

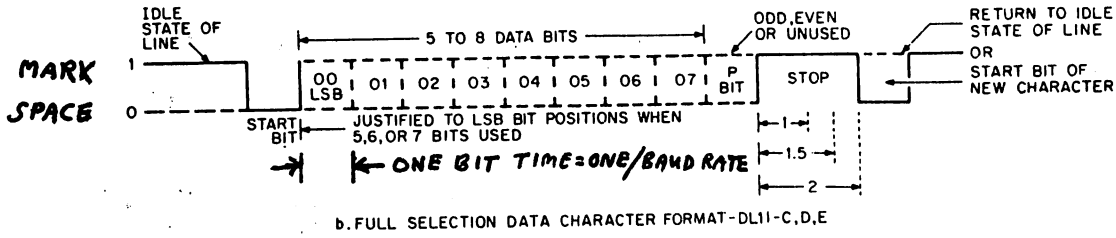
Table 2-3

Active - Passive Mode Selection

Transmitter	S1-1	S1-2	S1-3	S1-6	S1-7
Active	ON	ON	OFF	OFF	ON
Passive	OFF	OFF	ON	ON	OFF
Receiver	S3-6	S3-7	S3-8	S3-9	S3-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF
Reader Enable	S1-4	S1-5	S1-8	S1-9	S1-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

2.3 DATA FORMAT

The data format (Figure 2-2) consists of a START bit, five to eight DATA bits, a PARITY bit or no PARITY bit, and one, one and one-half, or two STOP bits.



b. FULL SELECTION DATA CHARACTER FORMAT-DL11-C,D,E

Figure 2-2 DL11-W Data Format

When less than eight DATA bits are selected, the hardware justifies the bits into the least significant bit positions for characters received by the interface. When transmitting characters, the program provides the justification into the least significant bits. The PARITY bit may be either on or off; when on, it can be selected for checking either odd or even parity during receive and for providing an extra PARITY bit during transmit.

All variable items within any data format are selected by switches on the DL11-W module. None of the variables can be controlled by the program. These switches are listed in Table 2-4 and described more fully in Chapter 5.

Table 2-4

Data Format Switches

NAME	SWITCH	UART PIN NO.	FUNCTION
No Parity	S4-6	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select (S4-2) switch. When disabled, the STOP bits immediately follow the last DATA bit during transmission. During reception, the receiver does not check for parity. Switch ON = parity enabled. Switch OFF = parity disabled.
Even parity	S4-2	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. Switch ON = odd parity. Switch OFF = even parity.
STOP Bit	S4-5	36	Selects the desired number of stop bits. Switch ON = 1 stop bit. Switch OFF = 2 stop bits, if 5 Data bits are selected 1.5 Stop bits will be selected.
Number of Data bits	S4-3 S4-4	38 37	These two switches are used together to provide a code that selects the desired number of DATA bits in the character. S4-4 S4-3 No. of DATA bits ON ON 5 ON OFF 6 OFF ON 7 OFF OFF 8

2.4 FUNCTIONAL DESCRIPTION

The DL11-W is, first, a character-buffered communications interface that performs two basic operations, receiving and transmitting asynchronous serial data and, second, a line frequency clock, used to measure time. As a receiver of serial data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the Unibus. This parallel character can then be gated through the bus to memory, a processor register, or some other device. As a transmitter, a parallel character from the bus is converted to a serial character for transmission to an external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operates through two related registers: a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or external device. The line frequency clock uses a signal derived from the A_C input voltage by the power supply to generate timed interrupts. The clock portion utilizes a register for command and monitoring functions.

Typically, the DL11-W is operated in one of two functionally different configurations. The DL11-W used as a Teletype control and the DL11-W used with EIA level converters will be discussed individually in the following paragraphs. The real-time clock functions will also be described.

2.4.1 DL11-W Teletype Control

The DL11-W (Figure 2-3) can be used to interface to Model 33, Model 35, and Model 38 Teletypes.

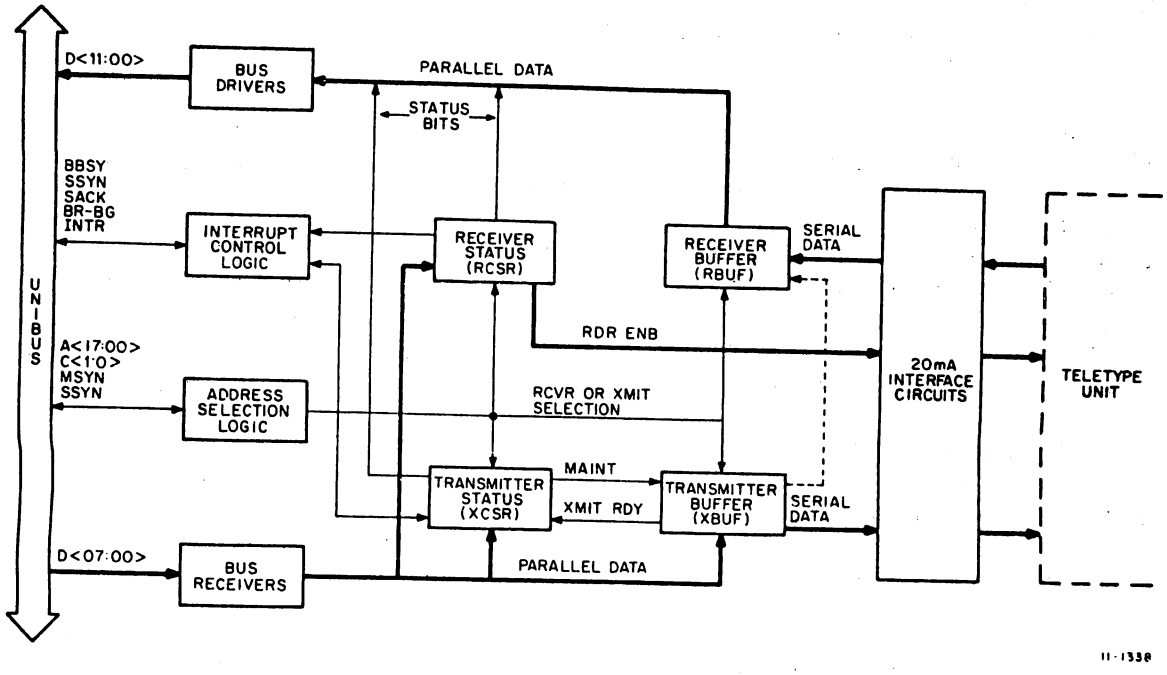


FIGURE 2-3
DL11-W TELETYPE CONTROL

serial information read or written by the teletype unit is assembled or disassembled by the DL11-W interface for parallel transfer to or from the Unibus. When the processor addresses the bus, the DL11-W interface decodes the address to determine if the Teletype is the selected external device and, if selected, whether it is to perform an input (read) or output (write) operation.

If for example, the Teletype has been selected to accept information for printout, parallel data from the Unibus is loaded into the DL11-W transmitter (punch) buffer. At this point, the XMIT RDY flag drops because the transmitter (punch) logic has been activated. (The flag comes back after a fraction of a bit time if the transmitter is not presently active.) The interface generates a START bit, shifts the data from the buffer into the teletype one bit at a time, again sets the XMIT RDY flag (as soon as the holding register of the double-buffering is empty, even through the shift register is active), and then times out the required number of STOP bits.

Thus, if the DL11-W is interfaced to a model 33 Teletype, the 8-bit parallel bus data is converted to the 11-bit serial input required by

the teletype. Note that, whenever a series of characters is to be loaded into the Teletype, the XMIT RDY flag is set prior to generation of the STOP bits and the shifting out of the character in the holding register, thus allowing another character to be loaded from the bus as soon as the transmitter holding buffer is empty. The XMIT RDY flag is used with XMIT INT ENB to initiate an interrupt sequence to inform the processor that the interface is ready to transfer another character to the Teletype for printing.

When receiving data from the Teletype unit, the operation is essentially the reverse. The START bit of the Teletype serial data activates the interface receiver logic, and data is loaded one bit at a time into the reader buffer register. When loading of the buffer is complete, the buffer contents are transferred to the holding register and the interface sets the RCVR DONE flag, indicating to the program that a character has been assembled and is ready for transfer to the bus. The RCVR DONE flag, if RCVR INT ENB is also set, initiates an interrupt sequence, thereby causing a vectored interrupt.

The DL11-W has a reader enable (RDR ENB) bit that can be set to advance the paper tape reader in the Teletype. When set, this bit clears the RCVR DONE flag. As soon as the Teletype sends another character, the START bit clears the RDR ENB bit, thus allowing just one character to be read.

The DL11-W also has a receiver active (RCVR ACT) bit, which indicates that the DL11-W interface is receiving data from the Teletype. This bit is set at the center of the START bit, which is the beginning of the input serial data, and is cleared by the leading edge of the RCVR DONE bit. The DL11-W also has a BREAK bit (can be switch-enabled), which can be set by the program to transmit a continuous space to the Teletype.

The DL11-W can be operated in a maintenance mode, which is selected by the program by setting the MAINT bit in the transmitter status register. When in this mode, special logic is used to perform a closed loop test of interface logic circuits. A character from the bus is loaded in parallel into the transmitter (punch) buffer register. The serial output of the register enters the receiver (reader) buffer register, where it is converted back into parallel data and transferred to the bus. In maintenance mode the data is not transmitted to the Teletype. If the DL11-W is functioning properly, the character in the reader buffer (RBUF) is identical to the character loaded into the transmitter buffer (XBUF).

2.4.2 DL11-W EIA Terminal Control

The DL11-W (Figure 2-4) also provides the control logic required for interfacing EIA terminals such as the VT06 Display or the Model 37 Teletype.

Functionally, the EIA Terminal control configuration is nearly identical with the Teletype control configurations. In the EIA

Terminal Control configuration, EIA level converters on the DL11-W are used to change bipolar serial input data to TTL logic level and TTL logic level serial output to bipolar signals required by EIA terminals. EIA level outputs for the signals DATA TERMINAL RDY and REQ TO SEND are permanently strapped on. There is no equivalent EIA level signal generated for RDR ENB.

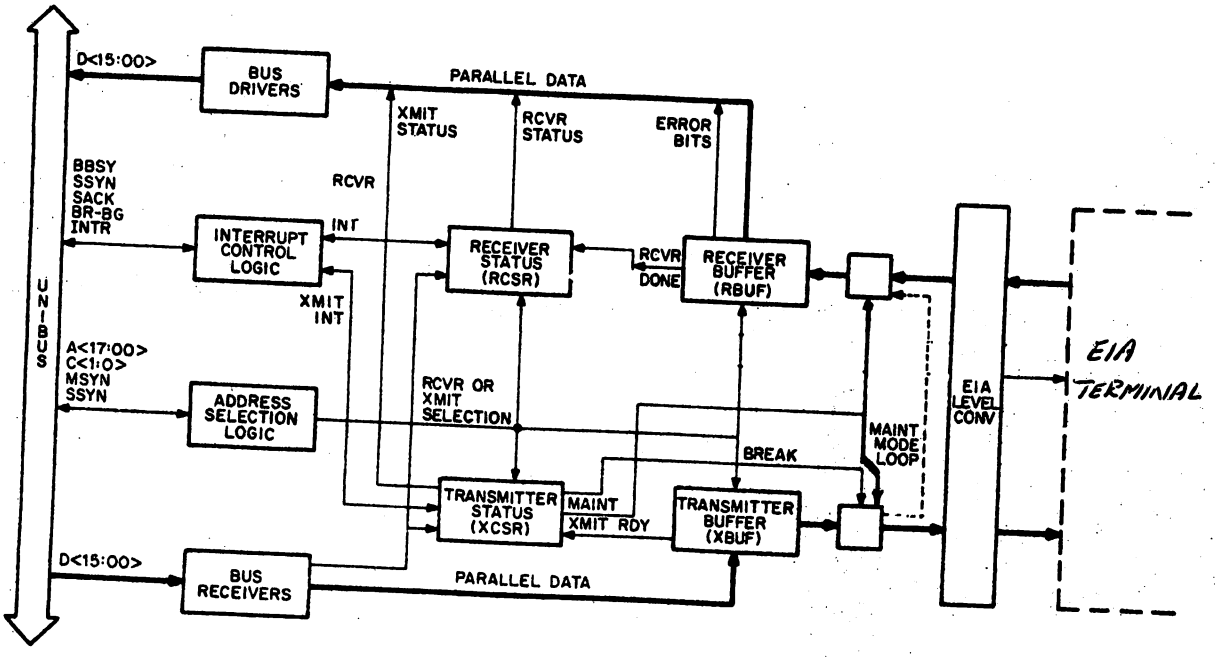


Figure 2-4 UL11-W EIA Terminal Control

2.4.3 Real-Time Clock

(Figure 2-5) A signal generated from the AC input line voltage by the power supply is received by the DL11-W. This signal is a square wave of identical frequency to the AC line voltage. A monitor bit (LTC MONITOR) is set once each cycle by the hardware but must be cleared by the program. By monitoring this bit, the program can count unit time intervals of 16 2/3 msec (60 Hz) or 20 msec (50 Hz). If the LTC INT ENB bit is set, a vectored interrupt will be generated each cycle.

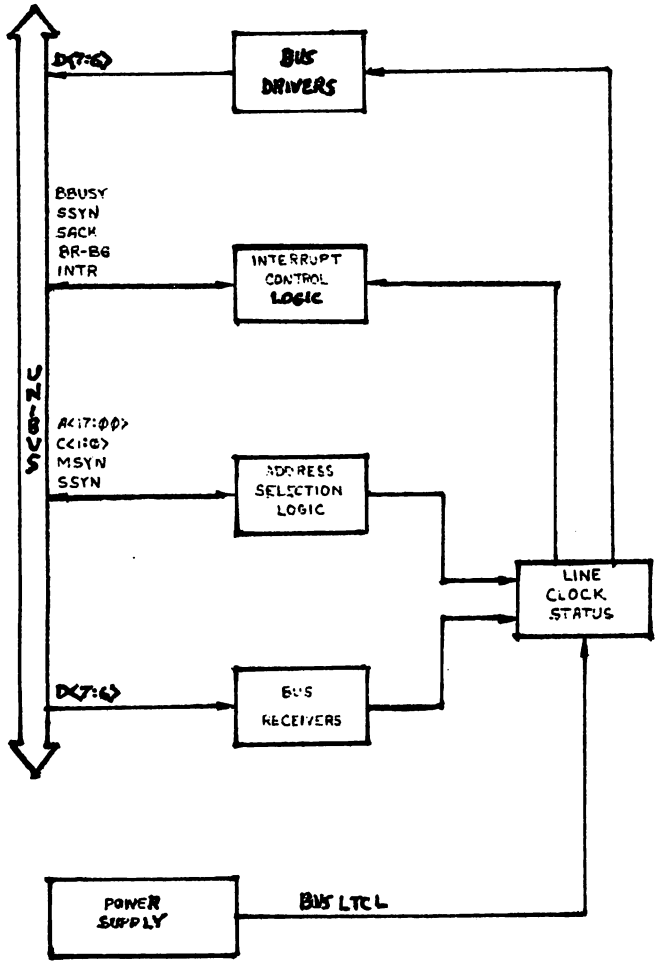


Figure 2-5 LINE CLOCK BLOCK DIAGRAM

2.5 PHYSICAL DESCRIPTION

The DL11-W SLU/RTC option is packaged on a single M7856 Quad Integrated Circuit Module that can easily be plugged into either a small peripheral controller slot in the processor or one of the four slots in a DD11-A Peripheral Mounting Panel. When the DD11-A is used, up to four DL11-W Interfaces can be mounted in a single system unit.

Power is applied to the logic through the power harness already provided in the BA_{11} Mounting Box. The required current is approximately 2.0A at +5V and 120MA at -15V. If the EIA level outputs are used, then $50MA$ of current, at a level between +9V and +15, is also required.

The M7856 module has a Berg connector for all user input/output signals. The specific signals fed to this connector depend on the external device interfaced to, and the specific cable used. Mounting, cabling, and connector information is given in Chapter 3.

Figure 2-6 shows the position of the Berg Connector and the five switch packs.

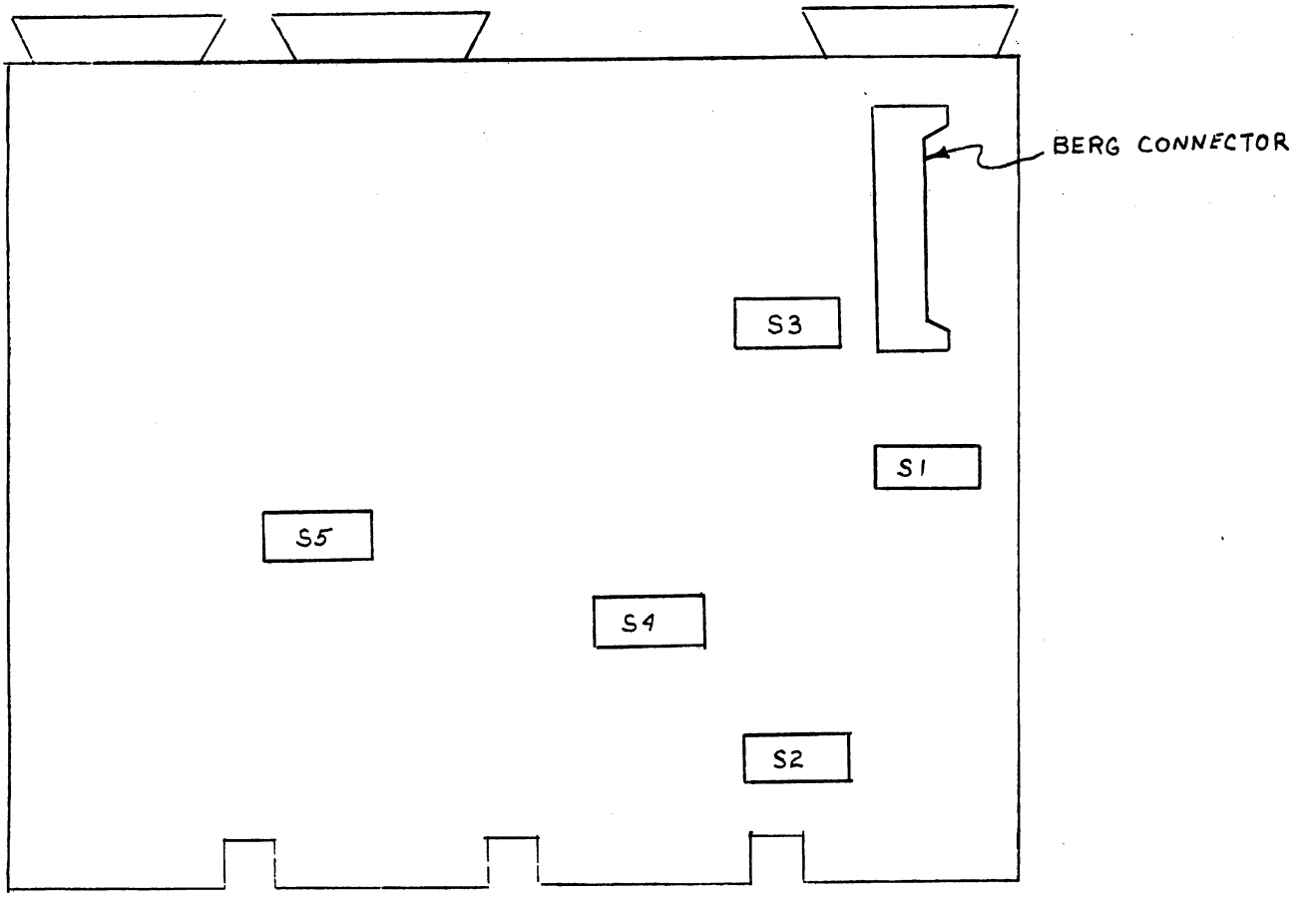


Figure 2-6 Position of Berg Connector and Switch Packs

2.6 SPECIFICATIONS

Operating and physical specifications for the DL11-W Serial Line Unit/Real-Time Clock are given in Table 2-5.

Table 2-5
DL11-W OPERATING SPECIFICATIONS

Specification	Description
Registers	Receiver Status Register (RCSR) Receiver Buffer Register (RBUF) Transmitter Status Register (XCSR) Transmitter Buffer Register (XBUF) (LKS)
Register Addresses	RCSR 777560 RBUF 777562 when used as console XCSR 777564 XBUF 777566 LKS 777546 VALID ONLY WHEN SLU USED AS CONSOLE RCSR 776XX0 RBUF 776XX2 XX=50 through 67 for up XCSR 776XX4 to 16 interfaces XBUF 776XX6 RCSR 77XXX0 RBUF 77XXX2 XXX=561 through 617 for XCSR 77XXX4 up to 31 interfaces XBUF 77XXX6
Interrupt Vector Address	060 receiver when used as console 064 Transmitter 100 - line clock Floating Vectors (Appendix B)
Priority Level	BR4 - SLU BR6 - RTC
Interrupt Types	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor
Commands	Receiver Interrupt Enable (RCVR INT ENB) Transmitter Interrupt Enable (XMIT INT ENB)

	Line Clock Interrupt Enable (LKS INT ENB) Reader Enable (RDR ENB) Maintenance Mode (MAINT) Break (BREAK)
Status Indications	Receiver Active (RCVR ACT) Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor Error (ERROR) Overrun (OR ERR) Framing Error (FR ERR) Parity Error (P ERR)
Data Input Output	Serial data, 20-MA active current loop. Serial data, 20-MA passive current loop. Serial data, conforms to EIA and CCITT specifications.
Data Format	1 START bit; 5, 6, 7, 8 bit DATA character; PARITY bit (odd, even, or unused); 1 or 2 STOP bits with 6, 7, 8 DATA bits, 1 or 1.5 STOP bits with 5 DATA bits.
Data Rates	Baud rates may be 110, 150, 300, 600, 1200, 2400, 4800, or 9600. Any split speed combination possible.
Bit Transfer Order	Low-order bit (LSB) first.
Parity	Computed on incoming data or inserted on outgoing data, dependent on type of parity (odd or even) used. Parity may be odd, even, or unused.
Size	Consists of a single quad module (M7856) that occupies 1/4 of a DD11-A or one of two controller slots in a KA11, KC11, or other PDP-11 processor system unit.
Power Required	2.0A at +5V 150MA at -15V 50MA at level between +9V and +15V.

The DL11-W does not include a cable; these must be purchased separately. Recommended cables are 7008360, for use when interfacing via 20-Ma current loop, and the BC05C-25 cable, for interfacing to EIA level devices.

Chapter 3

Installation and Configuration

3.1 INTRODUCTION

This chapter describes the physical components which constitute the DL11-W SLU/RTC Option and methods of mounting and connecting the DL11-W to other devices. This chapter is divided into three major parts; configuration, installation, and cabling.

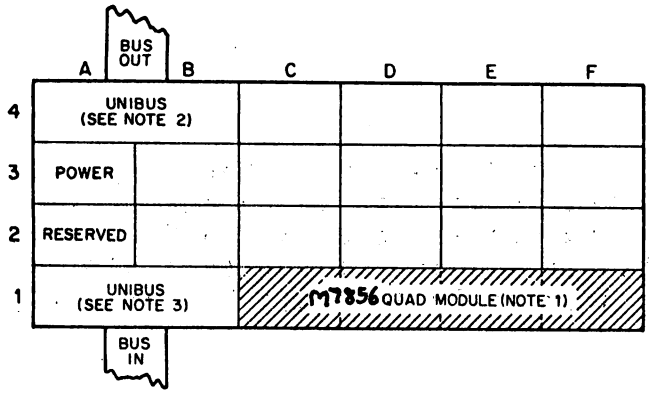
3.2 CONFIGURATION

The DL11-W option consists of an M7856 quad module.

Setup of switch selectable functions, baud rates, address and vector, and choice of cable will depend on system configuration programming considerations, and the external device being interfaced to.

3.3 INSTALLATION

The DL11-W interface can be mounted in either a small peripheral controller slot in the PDP-11 processor or in one of the four slots in a DD11-B Peripheral Mounting Panel, as shown in Figure 3-1. Note that the DL11-W can be mounted in any one of the four slots and up to four DL11-W interfaces can be mounted in a single system unit.



NOTES:
1. Can be mounted in slot 1, 2, 3 or 4
2. Can be M920, BC11-A, or M930
3. Can be M920 or BC11-A

Figure 3-1 DL11-W (M7856 Module) Mounted in DD11-B

A DL11-W interface can also be mounted in one of the four slots of a BB11 system unit, provided that the slot has been wired as a QD11-B or equivalent. See Table 3-1 for a list of signals and pin connections used. Once the M7856 module has been installed, an appropriate cable must be connected as described in Paragraph 3.4.

3.3.1 Power Connections

Power connections to the DL11-W interface are provided by the associated PDP-11 system via the power supply in the BA11 mounting box. When power is applied to the PDP-11 system, the DL11-W receives power also. These power connections are described in detail in the PDP-11 Peripherals and Interfacing Handbook, DEC, 1972.

When operating the EIA drivers, a positive voltage between 9v and 15v is required by the DL11-W. For PDP-11/15 and PDP-11/20 systems with an H720 Power Supply, a G8000 module must be installed to provide this voltage.

Table 3-1

SPC SLOT PINS AND SIGNALS USED BY THE DL11-W

SIGNAL NAME	PIN
BUS A00 L	EH2
BUS A01 L	EH1
BUS A02 L	EF1
BUS A03 L	EV2
BUS A04 L	EU2
BUS A05 L	EV1
BUS A06 L	EU1
BUS A07 L	EP2
BUS A08 L	EN2
BUS A09 L	ER1
BUS A10 L	EP2
BUS A11 L	EL1
BUS A12 L	EC1
BUS A13 L	EK2
BUS A14 L	EK1
BUS A15 L	ED2
BUS A16 L	EE2
BUS A17 L	ED1
BUS BUSY L	FD1
BUS BG4 IN H	DS2
BUS BG4 OUT H	DT2
BUS BG6 IN H	DM2
BUS BG6 OUT H	DN2
BUS BR4 L	DH2

BUS BR6 L	DE2
BUS C0 L	EJ2
BUS D1 L	EF2
BUS D00 L	CS2
BUS D01 L	CR2
BUS D02 L	CU2
BUS D03 L	CT2
BUS D04 L	CN2
BUS D05 L	CP2
BUS D06 L	CV2
BUS D07 L	CM2
BUS D08 L	CL2
BUS D09 L	CK2
BUS D10 L	CJ2
BUS D11 L	CH1
BUS D12 L	CH2
BUS D13 L	CF2
BUS D14 L	CE2
BUS D15 L	CD2
BUS INIT L	DL1
BUS INTR L	FM1
BUS LTC L	CD1
BUS MSYN L	EE1
BUS NPR L	EJ1
BUS SACK L	FT2
BUS DCLO L	CN1
BUS SSYN L	EJ1
BUS BG5 IN H	DP2**
BUS BG5 OUT H	DR2**
BUS BG7 IN H	DK2**
BUS BG7 OUT H	DL2**
+5V	CA2
	DA2
	EA2
	FA2
+15V	CU1
-15V	DB2
GND	CC2
	CT1
	DC2
	DT1
	EC2
	ET1
	FC2
	FT1

** Interconnected to provide bus grant continuity.

This module uses a filter network to convert the full-wave rectified +8V/rms signal to a positive dc voltage. Installation of the G8000 module is performed as follows:

1. Install the G8000 module into slot A02 of the DD11-A.

2. Connect wire between A03V2 and A02V2.

3. Connect a wire between A02N2 and CXXU1 (where XX is the slot location of the M7856 module).

3.3.2 Address Assignments

The DL11-W interface is addressed through the address selection logic and its interrupt vector, determined by the interrupt control logic. Each specific DL11-W interface within a system has a unique address and vector, both determined by the switches on the M7856 module, with the exception of the line clock address and vector, which are 777546 and 100 respectively. The addressing scheme is described is paragraph 5.2 and the vector address (interrupt control) scheme is covered in Paragraph 5.5.

3.3.3 Installation Testing

Installation testing is performed by running the appropriate diagnostic program after the DL11-W interface has been completely installed.

This program is contained on the diagnostic tape supplied with the interface. Instructions for running the diagnostic are included with the program tape.

Depending on the device used, the following diagnostics are supplied.

a.	DL11-W	MAINDEC-11-DZDLA
		MAINDEC-11-DZKWA
b.	Teletype	MAINDEC-11-DZKLA
c.	VT05	MAINDEC-11-DXVTB
d.	LA30	MAINDEC-11-DZLAB

3.4 CABLING

Figure 3-2 illustrates the method of connecting cables between the DL11-W and various external devices.

Table 3-2 lists the signal names and associated pins on the Berg connector mounted on the M7856 module. This table also lists the signals supplied on the 7008360 and BC05C cables.

Table 3-3 provides a quick reference of M7856 input/output signals for TTL, EIA, and 20-ma current loop devices.

Table 3-4 lists connector pin numbers and signals for the 7008360 cable.

Table 3-5 lists connector pin numbers and signals for the 7008519 cable which is used in conjunction with the 7008360 cable.

Table 3-6 lists connector pin numbers for the BC05C cable connectors.

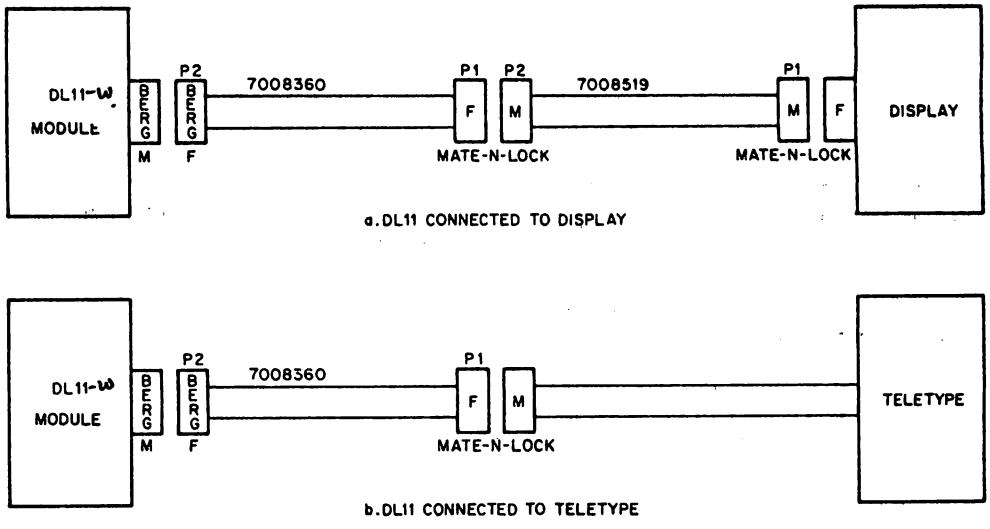


Figure 3-2 DL11-W Cable Connections

Table 3-2

Pin Connections

Berg Pin	M7856 Module	BC05C Modem Cable	7008300 Cable
A	Ground	Ground	Ground
B	Ground	Ground	
C		Force Busy	
D		Sec, Clear to Send	
E	Serial Input (TTL)	Interlock In	Interlock In
F	Serial Output (EIA)	Transmitted Data	
H	20 mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	Serial Input-(20 mA)		Received Data-
L		External Clock	
M	EIA Interlock	Interlock Out	
N		Serial Clock Xmit	
P		Sec, Request to Send	
R		Serial Clock Rcvr	
S	Serial Input-(20 mA)		Received Data-
T		Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W		-Power	
X		Ring	
Y		+Power	
Z		Data Set Ready	
AA	Serial Output+(20mA)		Transmitted Data+
BB		Carrier	
CC			
DD	Data Terminal Rdy (EIA)	Data Terminal Ready	
EE	Reader Run-(20 mA)		Reader Run-
FF		202 Sec, Xmit	
HH			
JJ		202 Sec, Rcvr	
KK	Serial Output-(20 mA)		Transmitted Data-
LL		EIA Sec, Xmit	
MM		Signal Quality	
NN		EIA Sec, Rcvr	
PP	Reader Run+(20 mA)		Reader Run+
RR		Signal Rate	
SS			
TT	+5V		
UU	Ground	Ground	Ground
VV	Ground	Ground	Ground

Table 3-3

Input/Output Signals

Type		Signals	Pin No.
TTL Signals	INPUT	Serial Data	E
20-mA current Loop signals	INPUT	+Serial Data	K
		-Serial Data	S
	OUTPUT	+Serial Data	AA
		-Serial Data	KK
		+Reader Run	PP
		-Reader Run	EE
EIA Signals	INPUT	Serial Data	J
	OUTPUT	Serial Data	F
		Request to Send	V
		Data Terminal Ready	DD

Table 3-4

7005360 Connections

Twisted Pair	Color	Mate-N-Loc Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Black/Red	Black	2	KK	-Transmitted Data
	Red	3	S	-Received Data
Black/White	Black	4	EE	-Reader Run
	White	5	AA	+Transmitted Data
Black/Green	Black	6	PP	+Reader Run
	Green	7	K	+Received Data
			E	Interlock In
			H	Interlock Out

NOTES: 1. Connector on ASR Teletype uses all pins (2-7).

2. Connector on KSR Teletype does not use pins 4 or 6 (Reader Run - and +).

Table 3-5
7008319 Connections

7008360 Mate-N-Lok Connector P1	Mate-N-Lok Connector P2 (To 7008360)	Color	Mate-N-Lok Connector P1 (To Device)	Signal
2	2	Black	2	-Transmitted Data
3	3	Red	3	-Received Data
4				
5	5	White	5	+Transmitted Data
6				
7	7	Green	7	+Received Data

Table 3-6
BC05C Connections

Color	Cinch Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Blue/White	1	A	Ground
		VV	Ground
White/Blue	2	F	Transmitted Data
Orange/White	3	J	Received Data
White/Orange	4	V	Request to Send
Green/White	5	T	Clear to Send
White/Green	6	Z	Data Set Ready
Brown/White	7	B	Ground
		UU	Ground
White/Brown	8	BB	Carrier
Slate/White	9	Y	+Power
White/Slate	10	W	-Power
Blue/Red	11	FF	202 Secondary Transmit
Red/Blue	12	JJ	202 Secondary Receive
Orange/Red	13	D	Secondary Clear to Send
Slate/Red	14	LL	EIA Secondary Transmit
Slate/Green	15	N	Serial Clock Transmit
Red/Brown	16	NN	EIA Secondary Receive
Slate	17	R	Serial Clock Receive
Red/Slate	18	U	Unassigned
Blue/Black	19	P	Secondary Request to Send
Black/Blue	20	DD	Data Terminal Ready
Orange/Black	21	MM	Signal Quality
Black/Orange	22	X	Ring
Green/Black	23	RR	Signal Rate
Brown/Red	24	L	External Clock
Red/Orange	25	C	Force Busy
		E	Interlock In
		M	Interlock Out

Table 3-3 provides a quick reference of M7800 input/output signals for TTL, EIA, and 20-mA current 1 devices.

Table 3-4 lists connector pin numbers and signals for the 7008360 cable.

Table 3-5 lists connector pin numbers and signals for the 7008519 cable connector which is used in conjunction with the 7008260 cable.

Table 3-6 lists connector pin numbers for the BC05C cable connectors.

Chapter 4

Programming Information

4.1 SCOPE

This chapter presents general programming information for software control of the DL11-W Serial Line Unit/Real-Time Clock Option. For more detailed information on programming in general, refer to the Paper-Tape Software Programming Handbook (DEC-11-GGPB-D).

This chapter of the manual is divided into three major portions: device registers, interrupts, timing considerations.

4.2 DEVICE REGISTERS

All software control of the DL11-W SLU/RTC Option is performed by means of five device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction referring to their addresses. Address assignments can be changed by altering the setting of switches on the address selection logic to correspond to any address within the range of 774000 to 777777. However, register addresses for the DL11-W normally fall within the range of 775610 to 776177 or 776500 to 776677. An explanation of the addressing scheme is offered in Chapter 5 of this manual. For the remainder of this discussion, it is assumed that the DL11-W is being used as a console terminal control.

The five device registers and associated bus addresses are listed in Table 4-1.

Table 4-1

Standard DL11-W Register Assignments

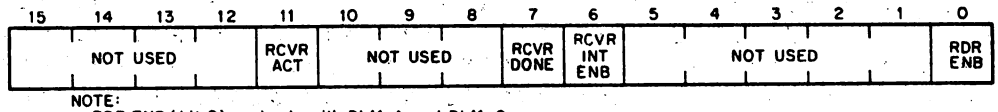
Register	Mnemonic	Address*
Receiver Status Register	RCSR	777560
Receiver Buffer Register	RBUF	777562
Transmitter Status Register	XCSR	777564
Transmitter Buffer Register	XBUF	777566
Line Clock Status Register	LKS	777546**

* These addresses are only for a DL11-W used as console terminal control. For other address assignments for these registers refer to Table 5-2.

** This address is valid only on a DL11-W used as console terminal. On any other DL11-W's used in system, this register should be disabled.

Figures 4-1 through 4-5 show the bit assignments for the device registers. The unused and read-only bits are always read as 0's. Loading unused or read-only bits has no effect on the bit position but should not be considered good programming practice. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction depressing the START switch on the processor console or the occurrence of a power-up or power-down condition of the processor power supply.

In the following descriptions, "transmitter" refers to those registers and bits involved in accepting a parallel character from the Unibus for serial transmission to the external device; "receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the Unibus.



NOTE:
RDR ENB (bit 0) used only with DL11-A and DL11-C
b.DL11-A THROUGH DL11-D OPTIONS

11-1342

Figure 4-1 RECEIVER STATUS REGISTER BIT FORMAT

Bit	Meaning and Operation
15 - 12	Unused.
11	RECEIVER ACTIVE -- Read only. When set, this bit indicates that the receiver interface is active. This bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and cleared by the leading edge of Receiver Done. Also may be cleared by INIT.
10 - 8	Unused.
7	RECEIVER DONE -- Read Only. Set when an entire

character has been received and is ready for transfer to the UNIBUS. Cleared by setting Reader Enable, addressing (READ or WRITE) RBUF, or INIT. Starts an interrupt sequence when RECEIVER INTERRUPT ENABLE (bit 6) is also set.

6 — RECEIVER INTERRUPT ENABLE -- Read/Write. Cleared by INIT. Starts an interrupt sequence when Receiver Done is set.

5 - 1 — Unused.

0 — READER ENABLE -- Write Only. Cleared by INIT or at middle of a START bit. Advances paper tape reader of ASR teletypes. Clears Receiver Done. 20mA current loop circuit output associated with this bit.

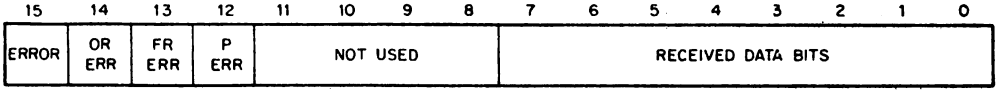


Figure 4-2 RECEIVER DATA BUFFER BIT FORMAT

Bit — Meaning and Operation

15 — ERROR -- Read Only. Logical OR of Overrun, Framing Error, and Parity Error. Cleared by removing the error conditions. ERROR is not tied to the interrupt logic, but Receiver Done is.

14 — OVERRUN -- Read only. Set if previously received character is not read (Receiver Done not reset) before the present character is received.

13 — FRAMING ERROR -- Read only. Set if the character read has no valid stop bit. Also used to detect break.

12 — RECEIVE PARITY ERROR -- Read Only. Set if received parity does not agree with the expected parity. Always 0 if no parity is selected.

NOTE: Error conditions remain present until the next character is received, at which time, the error bits are updated. INIT does not necessarily clear the error bits. Error bits may be

disabled via a switch, but not individually.

11,10,9,8	Unused.
7 - 0	RECEIVED DATA BITS -- Read Only. These bits contain the character just read. If less than 8 bits are selected, the buffer will be right-justified into the least significant bits, with the higher unused bit or bits reading as 0's. Not cleared by INIT.

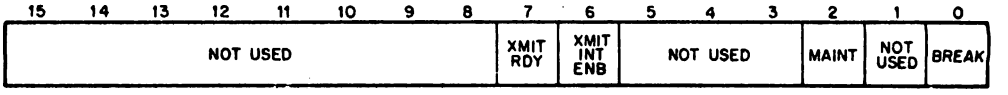


Figure 4-3 TRANSMITTER STATUS REGISTER BIT FORMAT

Bit	Meaning and operation
15 - 8	Unused.
7	TRANSMITTER READY -- Read Only. Set by INIT. Cleared when XBUF is loaded; set when XBUF can accept another character. When set it will start an interrupt sequence if Transmitter Interrupt Enable is also set.
6	TRANSMITTER INTERRUPT ENABLE -- Read/Write. Cleared by INIT. When set it will start an interrupt sequence if Transmitter Ready is also set.
5,4,3	Unused.
2	MAINTENANCE -- Read/Write. Cleared by INIT. When set, it disables the serial line input to the receiver and sends the serial output of the transmitter into the serial input of the receiver. Forces receiver to run at transmitter speed.
1	Unused.
0	BREAK -- Read/Write. Cleared by INIT. When set, it transmits a continuous space. May be disabled via a switch.

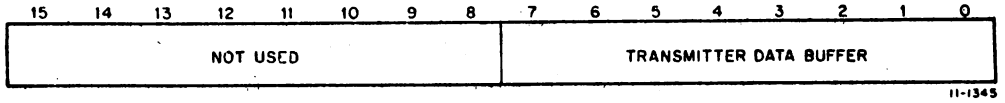


Figure 4-4 TRANSMITTER DATA BUFFER BIT FORMAT

Bit	Meaning and Operation
15 - 8	Unused.
7 - 0	TRANSMITTED DATA BUFFER -- Write Only. If less than 8 bits are selected then the character must be right-justified into the least significant bits.

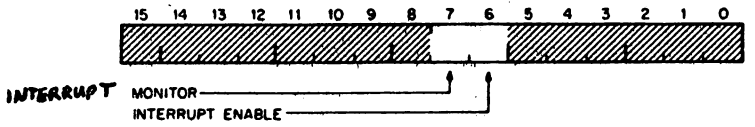


Figure 4-5 CLOCK STATUS REGISTER BIT FORMAT

Bit	Meaning and Operation
15 - 8	Unused.
7	LINE CLOCK MONITOR -- Read/clear. Set only by the line frequency clock signal and cleared only by the program. Set by INIT.
6	LINE CLOCK INTERRUPT ENABLE -- Read/Write. Cleared by INIT. When set, starts an interrupt sequence if Line Clock monitor is also set. An interrupt sequence will also be initiated upon the reception of the line frequency clock signal if the line clock monitor bit is

set from a previous clock signal.

5 = 0 Unused.

4.3 INTERRUPTS

The DL11-W interface uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing a branch to a handling routine. The DL11-W has three interrupt channels: one for the receiver section, one for the transmitter section, and one for the line clock section. These three channels operate independently; however, if simultaneous interrupt requests occur, the line clock has highest priority, followed by the receiver with the transmitter last.

A line clock interrupt can occur only if the LKS interrupt enable bit (bit 6) in the line clock status register is set. With LKS interrupt enable set, falling edges of the signal LTC IN L will generate interrupt requests. The signal LTC IN L is derived from the AC power input by the power supply and is a software wave of the same frequency as the AC input voltage.

A transmitter interrupt can occur only if the interrupt enable (XMIT INT ENAB) bit in the transmitter status register is set. With XMIT INT ENAB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. Setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus.

The interrupt priority level is 6 for the line clock and 4 for the receiver and transmitter.

The vector address for the line clock is fixed at 100, whereas floating vector addresses are used for the receiver and transmitter. The receiver vector is XX0 and the transmitter vector is XX4, where XX is assigned according to the method described in Paragraph 5.5. If the DL11-W is used as console terminal interface, then the receiver and transmitter vector addresses will be 60 and 64 respectively. The vector address can be changed by resetting switches in the interrupt control logic.

Any DEC programs or other software referring to the standard vector addresses must also be changed if the vector address is changed.

4.4 TIMING CONSIDERATIONS

When programming the DL11-W SLU/RTC option, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter, break generation logic, and line clock are discussed in the following paragraphs.

4.4.1 Receiver

The RCVR DONE flag (bit 07 in the RCSR) sets when the Universal Asychroneus Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double-buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

4.4.2 Transmitter

The transmitter section of the UART is also double-buffered. The XMIT RDY flag (bit 07 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

4.4.3 Break Generation Logic

When the BREAK bit (bit 00 in the XCSR) is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. However, because the transmitter section of the UART is double-buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudotransmitted character in the break should be null.

4.4.4 Line Clock

An initial synchronization period will be required when the LKS interrupt is initially turned on. In other words, the interval from setting LKS interrupt enable to the first interrupt will be some fraction of an AC power cycle period. All subsequent interrupts will occur at the proper intervals, depending upon the AC power frequency.

CHAPTER 5

DETAILED DESCRIPTION

5.1 INTRODUCTION

This chapter provides a detailed description of the DL11-W Serial Line Unit/Real-Time Clock Option. The discussions in this chapter are supported by a complete set of engineering drawings contained in a companion volume entitled DL11-W SLU/RTC Option, Engineering Drawings.

The complete DL11-W may be divided into 12 functional areas; each of these areas is covered separately in subsequent paragraphs. Table 5-1 lists each functional unit and the general purpose of each unit.

Table 5-1

DL11-W Functional Units

Functional Unit	Purpose
Selection Logic	Determines if the DL11-W interface has been selected for use and what type of operation (transmitter, receiver, or clock) has been selected. Permits selection of one of five internal registers and determines if the register is to perform an input or output function.
Register Logic	Five internal registers, addressable by the program, provide data transfer, command and control, and status monitoring functions for the interface.
Interrupt Request Logic	The line clock, receiver, or transmitter can request control of the Unibus for a vectored interrupt.

Interrupt Logic	Permits the DL11-W to gain control of the bus for a vectored interrupt.
Transmitter Control Logic	Provides necessary input control signals for the UART when it is used to convert parallel data from the Unibus to serial data required by the external device.
Receiver Control Logic	Provides necessary input control signals for the UART when it is used to convert serial data to parallel data required for transmission to the bus.
Universal Asynchronous Receiver/Transmitter (UART)	Performs the necessary serial-to-parallel or parallel-to-serial conversion on the data and supplies control and error detecting bits.
Baud Rate Logic	Determines the clock frequencies and, therefore, the baud rates for the transmitter and receiver sections of the UART. Eight baud rates are derived from a single oscillator and are independently switch-selectable.
Maintenance Mode Logic	Performs a closed-loop test of serial line unit control logic by tying the serial output of the transmitter into the receiver input, forcing the receiver clock to the same frequency as the transmitter clock.
Break Generation Logic	Permits the transmission of a continuous space on "break." The duration of the break can be timed by the pseudo-transmission of a specific number of characters.
20 MA Current Loop Logic;	Provides active or passive 20 MA current loops for use with 20 MA current loop devices;
EIA Logic	Provides necessary level

converters for use with EIA levels.

5.2 ADDRESS SELECTION

The address selection logic (drawings DL-4 & DL-7) decodes the incoming address information from the bus and provides the signals that determine which register has been selected and whether it is to perform an input or output function. Switches on the logic can be altered so that the module responds to any address within the range of 774000 to 777777. However, standard address assignments for the DL11-W normally fall within the ranges of 775610 to 776177 or 776500 to 776677.

The standard address assignments for DL11-W modules are listed in Table 5-2.

When the DL11-W is to be used as a console terminal control, switches are arranged so that the module responds only to standard device register addresses 77756m, 777562, 777564, 777566 and, if enabled, 777546. Although these addresses have been selected by DEC as the standard assignments for the DL11-W when used as a console terminal control, the user may change the switches to any address desired, with the exception of the line clock address which must be disabled. However, any MAINDEC program or other software that references these DL11 standard assignments must also be modified accordingly if other than the standard assignments are used.

TABLE 2-2

DL11-W STANDARD ADDRESS ASSIGNMENTS

UNIT	ADDRESS	REMARKS
CONSOLE	777560	
	777562	
	777564	
	777566	
	(777546)	LTC
UNIT #1	7776XX0	XX = 50 FOR UNIT #1
	7776XX2	51 FOR UNIT #2
	7776XX4	52 FOR UNIT #3
	7776XX6	!
		!
		!
UNIT #16		67 FOR UNIT #16
UNIT #17	77XXX0	XXX = 561 FOR UNIT #17
	77XXX2	562 FOR UNIT #18
	77XXX4	!
	77XXX6	!
		!
		!
UNIT #47		617 FOR UNIT #47

The DL11-W can be operated in one of three different address selection modes. Normally, a DL11-W used as console terminal control would operate in the first mode, whereas additional DL11s would be operated in the second mode. The third mode is not normally used, but is discussed here for completeness.

Mode 1: Both the serial line unit and the real-time clock sections can be addressed. Due to common address selection logic, operation in this mode requires that the serial line unit addresses be restricted to 77756X. The line clock address is 777546.

Mode 2: Only the serial line unit section can be addressed. Address selection ranges from 774000 to 777777. Line clock is disabled and does not respond to address 777546.

Mode 3: Only the line clock section can be addressed at 777546. The serial line unit section does not respond to any address.

Table 5-3 indicates the correct switch settings to select the desired address and address mode.

TABLE 5-3

ADDRESS AND MODE SELECTION

ADDRESS BIT	A10	A09	A08	A07	A06	A05	A04	A03	N/A	N/A
SWITCH	S5-3	S5-2	S5-1	S5-4	S5-5	S5-6	S5-8	S5-7	S5-9	S5-10
MODE 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
MODE 2 *	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
MODE 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

* Address 77756X selected for serial line interface. Other addresses may be selected using SWITCH=OFF = 1 and SWITCH=ON = 0.

The following discussions will assume that the DL11-W is operated as a console terminal control with the line clock enabled (mode 1).

The first five octal digits of the address 77756(X) indicate that the serial line unit has been selected to be used. The final octal digit (X), consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. To select the line clock register, 777546, the first 17 binary bits are decoded, and A00 is used to distinguish between a word or byte operation. In both cases, the two mode control lines C00 and C01 determine whether the selected register is to perform an input or output operation (provided that the selected register is a read/write register.)

The address decoding is performed by a series of logic gates that provide inputs to two 32 x 8 Read-Only Memory (ROM) IC chips. Basically, the state of the five input lines defines 1 of 32 unique addresses. The contents of the ROM corresponding to that unique address are then available at the output of the ROM. Each ROM provides 8 outputs, although only 14 of the 16 available outputs are used. Listings of the ROM contexts are provided in the engineering drawings.

One input to the ROMs is address bit A04 to decode the selection of the line clock or serial line unit. When the line clock is disabled, this line is always high. Two inputs, address bits A02 and A01, are used to select one of the four registers in the serial line unit and are also used in decoding the line clock address; the fourth input is a combination of A00, C00, and C01 providing necessary decoding of word or byte, input or output operations. The fifth input is an address enable which must be true for the ROMs to decode the other inputs. This address enable signal is derived from a series of gates that are true when MSYN is present and when the address line conditions indicate that one of the valid addresses is true on bus.

5.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 5-1. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the DL11-W is used, an OUT transfer is a transfer of data out of the master (the processor) and into the interface. Similarly an IN transfer is the operation of the interface furnishing data to the processor.

The address selection logic consists of 18 address lines (A<17:00>), 2 bus control lines (C<1:0>), and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 5-2. Note that all input gates are standard bus receivers.

1. Address lines A<17:11> must be all 1's. This specifies an address within the top 8K byte address boards for device registers.

2. Decoding of address lines A<10:05,03> is determined by switches. When a given line switch is ON, the address logic searches for a 0 on that line; if the switch is OFF, the logic searches for a 1. If only the serial line unit is to be enabled, then decoding of A04 will also be determined by a switch.

3. Lines A01, A02, and A04 are decoded to select one of the five addressable device registers.

4. Line C1 is decoded to select either an input (DATI) or output (DATO) function. When C1 is false an input (read) operation is selected; when it is true, an output (write or load) operation is selected.

5. Line A00 is used for byte control in such a manner that no register control signals are generated when a byte operation (DATOB) is performed on the high-order byte of any register.

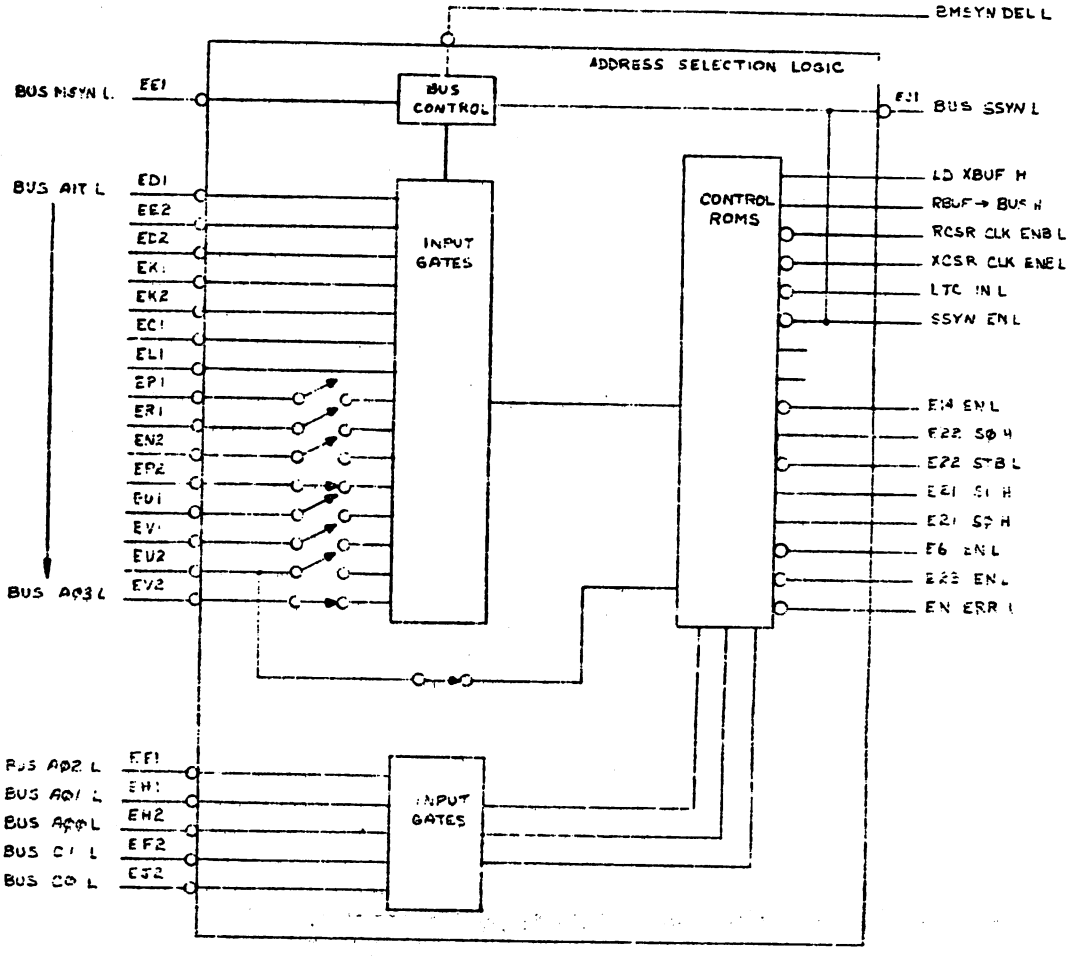


FIGURE 5-1 ADDRESS SELECTION LOGIC - SIMPLIFIED DIAGRAM

FIGURE 5-1 ADDRESS SELECTION LOGIC - SIMPLIFIED DIAGRAM

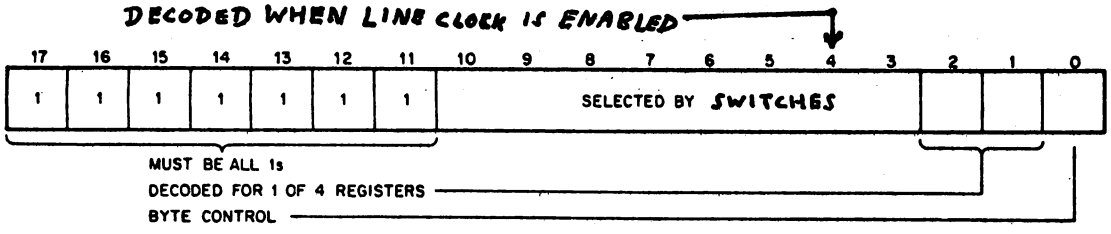


Figure 5-2 Interface Select Address Format

5.2.2 Outputs

The address selection logic output signals that are used permit selection of five 16-bit registers, and determine whether information is to be gated into or out of the master device. All of these output signals are listed in Table 5-4.

RCSR CLK ENB L and XCSR CLK EN L are ANDed with BMSYN DEL L to produce the register loading pulses RCSR CLK H and XCSR CLK H.

LD XBUF H is used to trigger a 500 nsec one-shot multivibrator to generate the transmitter buffer loading signals, LD X DEL L.

RBUF => BUS H triggers a 1 usec one-shot multivibrator to produce the signal SEL 2 L, which clears R DONE.

SSYN EN L is ANDed with BMSYN DEL L and delayed to produce BUS SSYN L.

TABLE 5-4

ADDRESS SELECTION LOGIC OUTPUT SIGNALS

SIGNAL	FUNCTION SELECTED	BUS CYCLE
LD XBUF H	Bus to transmitter buffer	DATO or DATOB*
RBUF->BUS H	Receiver buffer to bus	DATI or DATIP
RCSR CLK ENB L	Bus to receiver status	DATO or DATOB*
XCSR CLK ENB L	Bus to transmitter status	DATO or DATOB*
LTC IN L	Bus to line clock status	DATO or DATOB*
SSYN EN L	Returns BUS SSYN on a valid address selection	DATO, DATOB*, DATI, or DATIP
E14 E_N L	Enables bus drivers D01,D03,D04 and D05	DATI or DATIP
E22 S0 H	Selects either buffer (H) or transmitter status (L) to bus (bits 0 & 2)	DATI or DATIP
E22 STB L	Enables bits 0 & 2 (above) to bus drivers	DATI or DATIP
E21 S1 H E22 S0 H	Bits 6 and 7 of receiver buffer (S0=L, S1=L), receiver status (S0=L, S1=H), transmitter status (S0=H, S1=L), or line clock status (S0=H, S1=H) to bus.	DATI or DATIP
E6 EN L	Enables bus drivers D00, D02, D06, and D07	DATI OR DATIP
E23 EN L	Receiver status (bit 11) to bus.	DATI or DATIP
EN ERR L	Receiver buffer (bits 15,14,13, and 12) to bus.	DATI OR DATIP

* DATOB to low byte only (A00=0)

5.3 REGISTER LOGIC

All software control of the DL11-W is performed by five device registers. The registers are assigned Unibus addresses and can be read or loaded with any PDP-11 instructions that refer to their addresses (with certain exceptions such as load-only, read-only, or unused or disabled bits). Table 5-5 lists these registers and the function of each from a hardware standpoint. A discussion of the registers from a software standpoint is presented in Chapter 4.

5.3.1 Receiver Status Register (RCSR)

The receiver status register (RCSR) is used to monitor the status of receiver logic operations when the DL11-W accepts a character, and is used to initiate interrupt sequences.

Each of the bits in the receiver status register is discussed separately in the following paragraphs, beginning with the most significant bit.

5.3.1.1 Receiver Active (11) - The receiver active (RCVR ACT) flag indicates that the receiver logic is in the process of receiving and assembling an incoming character. This bit is read-only and is normally set and cleared by the receiver logic.

The RCVR ACT flag is set at the center of an incoming START bit by counting eight RCVR CLK periods from the beginning of a START bit. (XMIT CLK and RCVR CLK are 16 times the respective baud rates). RCVR ACT will remain set until the receiver done (RCVR DONE) flag is set.

TABLE 5.5

DEVICE REGISTER FUNCTIONS

Register	Mnemonic	Function
Receiver Status Register	RCSR	Provides detailed information on the status of the DL11-W receiver logic. Status information includes such flags as receiver active (RCVR ACT) and receiver done (RCVR DONE). Also includes the interrupt enable bit that can be used to initiate interrupt sequences when RCVR DONE sets.
Receiver Buffer Register	RBUF	Holds the character received from the external device prior to transfer to the Unibus. The format of the character is dependent on switch set-up. Four error bits that are set if a corresponding error condition arises during reading of a character from the device may be reported in the receiver buffer.
Transmitter Status Register	XCSR	Provides the interrupt enable bit and the transmitter ready (XMIT RDY) flag so that transmitter logic can be monitored and an interrupt sequence initiated, if desired. Provides the maintenance bit which can be set under program control to use the maintenance mode of operation. Provides a BREAK bit for generation of a continuous space.
Transmitter Buffer Register	XBUF	Holds the character to

		be transferred to the external device. Format of this data is dependent on the specific switch setup used.
Line Clock Status Register	LKS	Provides the interrupt enable bit and the line clock monitor bit to allow program monitoring of the line clock signal or timed interrupt sequences to be initiated if desired.

The RCVR ACT flip-flop is also cleared by BINIT L.

5,3,1,2 Receiver Done (Ø7) - The receiver done (RCVR DONE) flag indicates that a full character has been received. This bit, when set, clears the receiver active (RCVR ACT) flag and initiates an interrupt sequence provided the associated interrupt enable bit (RCVR INT ENB) is also set.

Once an entire character has been received and is stored in the UART holding register, the UART issues a received data available (R DONE) signal (Drawing DL-1) which is buffered and inverted and fed to the direct clear input of the RCVR ACT flip-flop to clear it, thereby indicating that the receiver is no longer in use and is capable of receiving a new character.

The buffered R DONE signal which becomes RCVR DONE H is ANDed with RCVR INTR ENB (1) H to produce a clock signal to set the receiver interrupt request flip-flop. The setting of this flip-flop will initiate an interrupt sequence as described in Paragraph 5. The RCVR DONE H signal is gated to the Unibus (Drawing DL-4) through a 411 multiplexer and through a bus driver enabled by the signals E6 EN L and BMSYN DEL L. This allows the status of the RCVR DONE bit to be read by the program from bus data line BUS DØ7 L.

The RCVR DONE bit can be cleared by INIT or by the occurrence of CLR R DONE. This signal occurs under two conditions. Whenever the read buffer (RUBF) is addressed, indicating that a new character may be loaded into the receiver, SEL 2 L is true and passes through an OR gate to produce CLR R DONE on the UART.

If the reader enable (RDR ENB) flip-flop is set, indicating that the tape reader in a Teletype unit is being advanced, then the Ø side is low and passes through the same OR gate as before to reset RCVR DONE.

5,3,1,3 Receiver Interrupt Enable (Ø6) - The receiver interrupt enable bit (RCVR INT ENB) permits an interrupt sequence to be initiated when the RCVR DONE bit sets, to indicate that a character has been received and is ready for transfer to the bus. This bit is set by using the RCSR CLK H signal as a load pulse to load a 1 from bus line BUS DØ6 L which is buffered to BBDØ6 H (Drawing DL-4) into the RCVR INTR ENB flip-flop (Drawing DL-1)

The output of the flip-flop, RCVR INTR ENB (1) H ANDed with RCVR DONE H clocks the receiver interrupt request flip-flop, setting it.

The RCVR INT ENB bit can be read onto the Unibus via the 411 multiplexer (Drawing DL-4) and through the bus driver enabled by E6 EN L and BMSYN DEL L onto bus data line BUS DØ6 L.

The RCVR INTR ENB flip-flop is cleared by BINIT L.

5,3,1,4 Reader Enable (ØØ) - The reader enable (RDR ENB) bit when set, advances the paper-tape reader in ASR Teletype units via a 2Ø MA output circuit. The BBD Ø H signal, which is derived from receiving BUS DØØ L, is applied to the data input of the RDR ENB flip-flop (Drawing DL-1); the clock input receives the loading signal RCSR CLK H. When the flip-flop is set, the Ø side which is low is applied to the 2Ø MA circuit (Drawing DL-5) which advances the paper-tape leader in the Teletype via pin PP on the Berg connector. The Ø side of the flip-flop is also gated through an OR gate (Drawing DL-1) to reset the RCVR DONE bit via CLR R DONE as described in Paragraph 5,3,1,2.

The RDR ENB bit is a write-only bit; it cannot be read by the program.

Whenever the Teletype starts sending data to the interface, the RDR ENB bit is cleared so that the reader does not advance another frame while it is transmitting information to the DL11-W.

The RDR ENB flip-flop is cleared when the RCVR ACT flip-flop becomes set, which is at the middle of a START bit as explained in Paragraph 5,3,1,1.

The RDR ENB flip-flop can also be cleared by BINIT L.

5,3,2 Receiver Buffer Register (RBUF)

The receiver buffer (RBUF) is an 8-bit read-only register in the UART. Serial information is converted to parallel data by the UART and then gated to the Unibus. The RBUF consists of gating logic rather than a flip-flop register; therefore, the data output lines from the UART must be held until read onto the bus. Because the UART is double-buffered, data on these output lines is valid until the next character is received and assembled. The RBUF register is read by a DATI sequence and the data is transmitted to the Unibus for transfer to the processor or some other PDP-11 device.

If less than 8 data bits are selected, the buffer is justified into the least significant bit positions. This justification is performed by the UART. The data loaded into the buffer is coded so that binary Ø's correspond to spaces and binary 1's correspond to marks (or holes).

The four most significant bits in the high-order byte of register are used for error indications. The error bits and the data portion of the receiver buffer register are covered separately in the following paragraphs.

5,3,2,1 Receiver Error Bits - (15, 14, 13, 12) - The high-order byte of the receiver buffer register (RBUF) contains four error bits that set to indicate improper receiver operation. These bits are read-only and can be disabled by having switch S4-7 in the OFF position.

Three of the four error bits are generated in the UART as follows:

1. OR ERROR = (overrun error, bit 14) = Indicates that R DONE was not reset (previously received character was not read) prior to receiving a new character. When this condition exists, the UART generates an OR ERR H signal.

2. FR ERROR = (framing error, bit 13) = Indicates that a framing error exists because the character read had no valid STOP bit. When this condition exists, the UART generates a FR ERR H signal.

3. P ERROR = (parity error, bit 12) = Indicates that the parity received does not agree with the expected parity. If parity has been selected and this condition exists, the UART generates a P ERR H signal.

Bit 15, which is the error (ERROR) bit, is the inclusive-OR of the OR ERROR, FR ERROR and P ERROR bits. Whenever one of these errors occurs, the appropriate signal from the UART (OR ERR H, FR ERR H, or P ERR H) passes through a buffer and qualifies an OR gate (Drawing DL-11). The output of the OR gate is ERROR H. Each of the four error signals (Drawing DL-4) qualifies one leg of a 2-input NAND gate. The other leg is qualified by BMSYN DEL L ANDed with EN ERR L. The output of each NAND gate is tied to an associated bus data line (BUS D15 L, BUS D10 L, BUS D13L, and BUS D12 L) so that the status of each error bit can be monitored by the program. Note that the enabling signal EN ERR L is applied via switch S4-7 and if this switch is off the error bits cannot be read onto the bus.

It should be noted that none of the error bits is tied to the interrupt logic. Therefore occurence of a receiver error does not cause the program to be interrupted for a branch to a handling routine. However, these flags are updated each time a character is received, at which point an interrupt may occur by means of R DONE.

The initialize signal (B INIT) may have an effect on these bit positions depending on the UART used. A bit is cleared by clearing the error-producing condition. When the next character is received by the UART, the error bits are updated and the new status available when the receiver buffer register is read.

5,3,2,2 Receiver Data Bits (07 through 00) = The receiver buffer register is not a flip-flop register, but consists simply of gates that strobe data from the output lines of the UART onto the Unibus. The UART receives the incoming serial data from the external device, converts it to parallel data, and places it on eight parallel output lines. Each of these lines (RD0 thru RD7) is fed to one leg of a NAND gate as shown on Drawing DL-4 (RD0 and RD2 through the 2:1 multiplexer; RD6 and RD7 through the 4:1 multiplexer). When the receiver buffer is addressed for reading, E14 EN L and E6 EN L will also be true and, ANDed with BMSYN DEL L, will gate the receiver buffer levels to bus data lines BUS D07 L through BUS D00 L.

Figure 5-3 is a simplified diagram of both receiver and transmitter gating logic showing a single bit position. When the receiver gating is used, the output of the UART is gated through to the Unibus. When the transmitter is used, data from the Unibus is gated through to the transmitter inputs of the UART.

The receiver buffer can only be read by the program. It is loaded by the UART. Note that the initialize signal (BINIT) has no effect on this register.

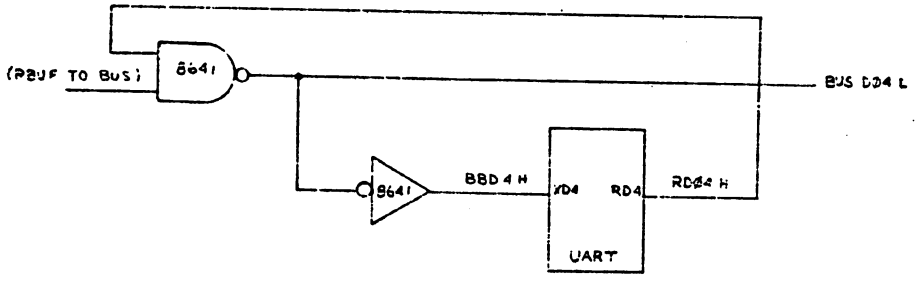


FIGURE 5-3 RBUF AND XBUF GATING LOGIC - SIMPLIFIED DIAGRAM

FIGURE 5-3 RBUF AND XBUF GATING LOGIC - SIMPLIFIED DIAGRAM

5,3,3 Transmitter Status Register (XCSR)

The transmitter status register (XCSR) consists of control and status monitoring bits for the transmitter portion of the DL11-W.

The transmitter status register contains two bits associated with transmitter operation: a transmitter ready flag to indicate that the transmitter buffer can be loaded, and an interrupt enable to allow the transmitter to initiate an interrupt sequence. Both of these bits are described in subsequent paragraphs.

A maintenance (MAINT) bit is also provided so that a closed-loop test of the serial line unit operation can be performed. The maintenance function is covered in detail in Paragraph 5.10 .

A BREAK bit (bit 00) is also provided and permits transmission of a continuous space to the external device. This bit may be disabled via a switch. The associated logic is described in Paragraph 5.10 .

5,3,3,1 Transmitter Ready (07) - The transmitter ready (XMIT RDY) flag indicates that the transmitter buffer (XBUF) is ready to accept another character from the Unibus for transfer to the external device. This bit, when set, initiates an interrupt sequence, provided the associated interrupt enable bit (XMIT INT ENB bit 06) is also set.

This bit is controlled by the XRDY output of the UART which indicates that the transmitter buffer is empty. It is set by the initialize signal (BINIT H) to indicate that the data bits holding register within the UART may be loaded with another character. It is also set whenever the holding register is empty. Once loading of the transmitter buffer begins, this bit is cleared. The XRDY output of the UART is buffered to produce XMIT RDY H flag.

As shown in Drawing DL-1, the XMIT RDY H signal is ANDed with XMIT INTR ENB (H) H which is true if bit 06 is set to clock the 7474 flip-flop setting it. The 0 side of this flip-flop, which is now low, is ANDed with XMIT INTR ENB (1) L, and the output of this gate initiates an interrupt sequence. The interrupt sequence allows the program to branch to a handling routine for loading a character for transmission to the external device.

The XMIT RDY flag can be read by the program from bus data line BUS D07 L via the 411 multiplexer and associated bus driver.

5,3,3,2 Transmitter Interrupt Enable (06) - The transmitter interrupt enable bit (XMIT INT ENB) permits an interrupt sequence to be initiated when the XMIT RDY bit sets to indicate that the transmitter buffer can accept another character from the Unibus. This bit is set by using XCSR CLK H as a load pulse to load a 1 from bus line BBD 6 H into the XMIT INTR ENB flip-flop (Drawing DL-1)

The output of the flip-flop, XMIT INTR ENB (1) H, is applied to one leg of a 2-input AND gate. The other input of this AND gate is the XMIT RDY H signal, which is produced when the transmitter buffer is clear and capable of receiving a character from the bus. When both inputs are true, the output clocks the 7474 flip-flop, initiating an interrupt sequence.

As shown on Drawing DL-4, the XMIT INTR ENB (1) H signal is applied to an input of the 411 multiplexer, which can be read onto bus data line BUS D06 L so that the program can read the status of this bit.

The XMIT INT ENB flip-flop is cleared by BINIT L.

5.3.4 Transmitter Buffer Register (XBUF)

The transmitter buffer (XBUF) is an 8-bit write-only register that receives the parallel character from the Unibus and loads it into the UART for serial conversion and transmission.

Some switch selections may cause the UART to be operated with a data format of less than eight data bits. In these cases, the data character must be justified into the least significant bit positions by the program. Bit positions within the UART itself are enabled or disabled according to the format code selected. Thus, for example, if a 5-bit code was selected, bit positions 5, 6, and 7 are disabled. If the program does not justify the character and is loaded into the most significant bit positions, data loaded into bits 5, 6, and 7 would be lost.

When the interface is initialized, the XMIT RDY flag is set to indicate that the XBUF can be loaded. When the buffer is loaded with the first character, the flag clears and then sets again within a fraction of a bit time. A second character can then be loaded because the UART transmitter section is double-buffered. When the second character is loaded, the flag clears again, but this time remains clear for nearly a full character time.

The transmitter buffer (Drawing DL-1) is not a flip-flop register, but consists of bus data buffers and a strobe pulse to load data from the Unibus to the input lines of the UART. Transfer of data is accomplished by a DATO or DATOB bus cycle.

The character to be transmitted to the device is loaded onto the bus data lines BUS D07 L through BUS D00 L and gated to the UART input lines as BBD 7 through BBD 0. Once on the input lines, the data is strobed into the UART by the LD X DEL L signal.

Figure 5-3 is a simplified diagram of both receiver and transmitter gating logic showing a single bit position.

Loading of the transmitter buffer is such that a logic 1 causes a mark (or hole) to be transmitted and a logic 0 causes a space.

5.3.5 Line Clock Status Register (LKS)

The line clock status register (LKS) consists of control and status monitoring bits for the line clock portion of the DL11-W.

The line clock status register contains two bits associated with line clock operation: a line clock monitor bit to provide non-interrupt mode timing information and an interrupt enable to allow the line clock to initiate an interrupt sequence. Both of these bits are described in subsequent paragraphs.

5.3.5.1 Line Clock Monitor (07) - The line clock monitor bit provides a program with a means of measuring a timed interval in a non-interrupt mode. The line clock monitor bit is set once each cycle of the input AC power into the machine. The program must clear the bit after noting that it was set each time.

As shown in Drawing DL-2, this bit is set by the power supply generated signal BUS LTC L on the clock input of flip-flop LTC BIT 07. BUS LTC L is a square-wave signal with the same frequency as the AC input power.

This flip-flop is cleared only by the program. This occurs when bus data line BUS D07 L has a logic 0 and is loaded into the line clock monitor bit (LTC BIT 07). The inverted bus data line (BBD 7 H) is again inverted (Drawing DL-2) and is ANDed with LTC IN L, BMSYN DEL L, and BSSYN L to generate a pulse which direct-clears the flip-flop LTC BIT 07. Note that if bus data line BUS D07 L had been a logical 1, the monitor bit would not have been set by the program. This bit can be read by a program via the 411 multiplexer and bus driver in Drawing DL-4.

This bit is set by B INIT L.

5.3.5.2 Line Clock Interrupt Enable (06) - The line clock interrupt enable bit allows the line clock portion of the DL11-W to generate timed interrupt sequences. Interrupt sequences would occur at time intervals of 16 2/3 msec (60 Hz) or 20 msec (50 Hz) depending upon the frequency of the AC input voltage.

A logical 1 on bus data line BUS D06 L is inverted and applied to the data input of the LTC BIT 06 flip-flop. The 1 is then loaded into the flip-flop, using the ANDed combination of BMSYN L and LTC IN L as a load pulse.

With LTC BIT 06 set, this would normally remove the direct clear signal from the interrupt request flip-flop. The next occuring falling edge of BUS LTC L from the power supply would clock the interrupt request flip-flop initiating and interrupt sequence.

LTC BIT 06 H can be read onto the bus data line BUS D06 L via the 411

multiplexer and bus driver (Drawing DL-4).

Line clock interrupt enable (LTC BIT 06) will be cleared by BINIT L.

5.4 INTERRUPT REQUEST LOGIC

The DL11-W contains two separate interrupt request logic circuits, one initiates interrupt sequences for the line clock portion and one initiates interrupt sequences for the serial line portion.

5.4.1 Line Clock

The line clock interrupt request logic consists of an interrupt request flip-flop and a bus driver (Drawing DL-2). The interrupt request flip-flop is set on the falling edge of the signal BUS LTC L. When set, the 1 side output enables one leg of a 2-input bus driver gate. The other input is enabled until the processor acknowledges the interrupt request. The bus driver enables the Unibus signal BUS BR 6 L, which initiates the interrupt sequence. The interrupt request flip-flop can be cleared by obtaining control of the bus (RTC MASTER L), by writing a 0 into LTC BIT 07, or if LTC BIT 06 is cleared.

5.4.2 Serial Line Unit

The interrupt request logic for the serial line unit consists of two interrupt request flip-flops (one for the receiver, one for the transmitter, an arbitrator circuit, and a bus driver.

The receiver interrupt request flip-flop (Drawing DL-1) is set by the ANDed conditions of RCVR DONE H and RCVR INTR ENB (1) H. The 1 side of this flip-flop is ANDed with RCVR INTR ENB (1) H to generate an interrupt request signal, which is applied to the arbitration circuit. The receiver interrupt request flip-flop can be cleared by one of the following conditions: BINIT L becomes bus master (MASTER H ANDed with RCVR INTR RQST H); or CLR R DONE is generated.

The transmitter interrupt request flip-flop (Drawing DL-1) is set by XMIT RDY H ANDed with XMIT INTR ENB (1) H or by BINIT L. When set, the 0 side output, which is low, is ANDed with XMIT INTR ENB (1) L to generate an interrupt request signal, which is applied to the arbitration circuit. This flip-flop can be cleared if the transmitter becomes bus master (MASTER H ANDed with XMIT INTR RQST H) or if the transmit buffer is loaded (LD X DEL L).

The function of the arbitrator circuit is to arbitrate simultaneous interrupt requests from both the receiver and transmitter. The arbitrator circuit has two inputs and two outputs. The two inputs are the gated outputs of the receiver interrupt request flip-flop and the transmitter interrupt request flip-flop. The outputs of the

arbitrator circuit are the two signals, RCVR INTR RQST H and XMIT INTR RQST H. Only one output is true at one time; generally the flip-flop which sets first generates the interrupt request.

5.5 INTERRUPT CONTROL LOGIC

The interrupt control logic permits the DL11-W to gain control of the bus (become bus master) and perform an interrupt operation. The DL11-W contains two separate interrupt controls, one for the line clock and one for the serial line unit. The vector for the line clock is fixed at 100 but the serial line unit vector may be altered via switches so that the logic has a normal address within the range of 000 to 776. However, the specific vector used with a particular DL11-W is dependent upon its use within a system.

The standard vector addresses for the DL11-W when used as a console interface are 060 and 064. Other DL11-Ws in the system are assigned "floating" vectors according to the addressing scheme given in Appendix B.

NOTE

The final octal digit of the vector address is not affected by the the switches; therefore, regardless of the vector address selected by the switches, the final octal digit is always 0 for the receiver and 4 for the transmitter.

Since both the line clock and serial line unit interrupt controls are basically the same, only the serial line unit interrupt control logic will be discussed in subsequent paragraphs. Figure 5-4 is a simplified diagram of the interrupt control logic.

The serial line unit interrupt control logic is shown on Drawing DL-3. If either a receiver interrupt request or transmitter interrupt request or both is generated, the arbitrator circuit in the interrupt request logic (Paragraph 5.4) will generate one of the two signals RCVR INTR RQST H or XMIT INTR RQST H. These two signals are ORed together and applied to one leg of the bus request driver on BUS BR4 L. The other leg is enabled if the interrupt control logic is not currently master (BUSY) or already the next master (SACK).

The processor will either respond to the bus request with bus grant or remove the conditions causing the DL11-W to issue the request (i.e., issuing a BUS INIT). Normally, the processor will continue the interrupt sequence by the issuance of BUS BG4 IN H. Because bus grants are "daisy-chained" from device to device, the DL11-W must decide either to accept the bus grant signal or to pass it on to the next device.

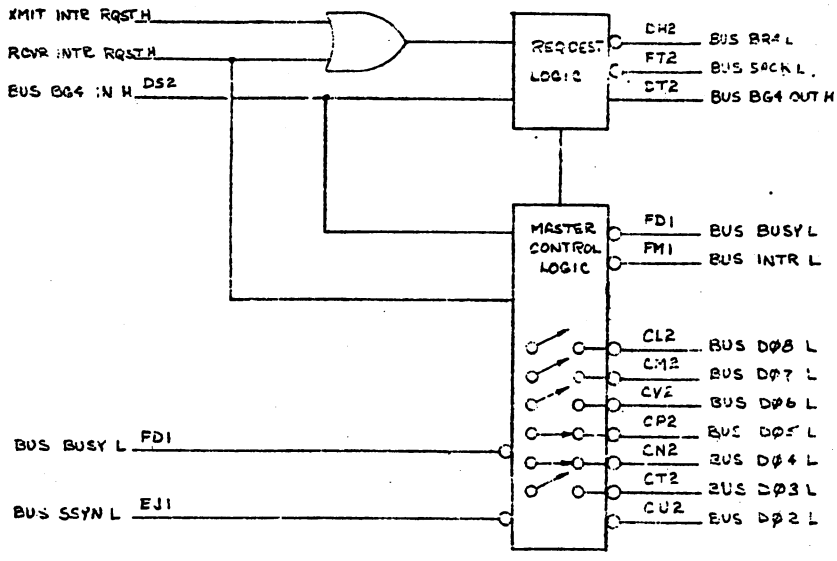


FIGURE 5-4 INTERRUPT CONTROL - SIMPLIFIED DIAGRAM

FIGURE 5-4 INTERRUPT CONTROL - SIMPLIFIED DIAGRAM

This decision is made by an arbitrator circuit such as that shown in the simplified diagram in Figure 2-5. Basically, if the serial line unit generates an interrupt request before the reception of the bus grant, the DL11-W will accept the grant and, if the request is raised after the grant, pass it on. The arbitrator will decide one way or the other when both events occur simultaneously. If the grant is passed on, then the bus driver on BUS B04 OUT H will be enabled. If the arbitrator circuit accepts the bus grant, then the grant accept signal is ANDed with bus grant to generate a set signal for the R-S SACK flip-flop. The SACK flip-flop enables the BUS SACK driver and, ORed with the BUSY flip-flop, disables the BUS BR4 driver. The processor will respond to the signal BUS SACK L by unasserting BUS B04 IN H.

With the assertion of BUS SACK L, the DL11-W is now prepared to become bus master when the bus becomes free. The data input of the BUSY flip-flop is primed with the 1 side of the SACK flip-flop. A clock edge is generated when the bus becomes free by the ANDed condition of BUS BUSY L, BUS SSYN L, AND BUS B04 IN. When the BUSY flip-flop is set, the 1 side output is applied to the BUS BUSY driver to signal that the bus is in use. The 0 side of the flip-flop, which is now low, is used as MASTER L, indicating that the interrupt control logic is now master of the bus.

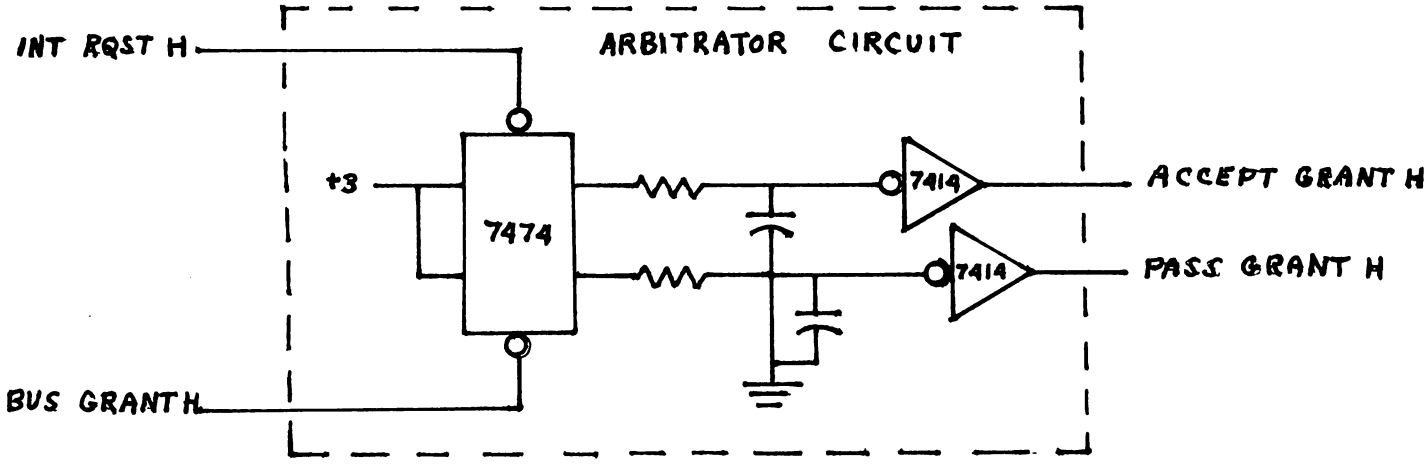


FIGURE 5-5

ARBITRATOR CIRCUIT

MASTER L is inverted and used to enable the vector address onto the Unibus and to assert BUS INTR L. The processor responds to BUS INTR L by asserting BUS SSYN L, which after being inverted by the bus receiver, clears the BUSY flip-flop.

BINIT H also clears both the SACK flip-flop and the BUSY flip-flop.

Note that a given vector address switch is ON for a 1 and OFF for a Ø.

5.6 TRANSMITTER CONTROL LOGIC

The transmitter control logic provides the necessary input, control, and output logic for the UART when it is used to convert parallel data from the Unibus to the serial data required for output. This logic may be divided into three functional areas: control and input, format selection, and data output.

The control and input logic for the transmitter portion of the UART consists of both input and output control signals, a clock frequency, and an input data character. These signals are listed in Table 5-6.

TABLE 3-6

TRANSMITTER CONTROL AND INPUT LOGIC

SIGNAL MNEMONIC	SIGNAL NAME	DESCRIPTION
XRDY	Transmitter Ready	The XMIT RDY flag that indicates the buffer is empty and may be loaded with another character from the Unibus.
LD XD	Load Transmitter Data	The signal that strokes data from the bus into the UART when the XBUF is addressed for loading.
XCLK	Transmitter Clock Pulse	Provides the required transmitter clock rate. This rate is 16 times the selected baud rate.
XD0-XD7	Data Buffer	Represents the character (five to eight bits) loaded from the Unibus into the UART.

The format selection logic basically consists of switches that are arranged to select the number of data bits, STOP bits, and type of parity. Format selection is covered in Table 5-7.

The output logic of the transmitter is described in the following paragraphs.

Once the UART has converted the parallel character from the Unibus (UART operation is described in Paragraph 5.8), it shifts the character out, one bit at a time onto the serial output (SERIAL OUT) line. The first bit shifted out is the START bit, followed by the DATA bits (LSB first), then the PARITY bit (if selected), and finally, the STOP bits. The output of the line passes through a NAND gate to produce SERIAL OUT L. This gate is used to generate a SPACE when the BREAK bit is used.

The SERIAL OUT L is connected to a circuit that converts the line to the bipolar levels required by the 20MA current loop (Drawing 0L-5). The resultant positive serial data is applied to pin AA of the Berg connector and the negative serial data is applied to pin KK.

SERIAL OUT L passes through an inverter and is applied to an EIA level converter to pin F of the Berg connector.

The inverter output SERIAL OUT H is also applied to the MAINT multiplexer circuit for use during maintenance mode as described in Paragraph 5.10.

TABLE 3-7

DATA FORMAT SWITCHES

Name	Switch	UART Pin No.	Function
No Parity	S4-6	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select switch (S4-2). When disabled, the STOP bits immediately follow the last DATA bit during transmission. During reception, the receiver does not check for parity. ON = parity enabled OFF = parity disabled
Even Parity	S4-2	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. ON = odd parity OFF = even parity
STOP Bit	S4-5	36	Used to select the desired number of STOP bits. 1 STOP bit = ON 2 STOP bits = OFF (except with 5 data bits) 1.5 STOP bits = OFF (with 5 data bits only)
Number of Data Bits	S4-3 S4-4	38 37	These two switches are used together to provide a code that selects the desired

number of DATA bits in the character.

S4-4	S4-3	No. of DATA Bits
ON	ON	5
ON	OFF	6
OFF	ON	7
OFF	OFF	8

5.7 RECEIVER CONTROL LOGIC

The receiver control logic provides the necessary input, output, and control logic for the UART when it is used to convert serial data to the parallel data required by the Unibus. This logic may be divided into three functional areas: status and control, format selection, and data input.

The status and control portion of the logic consists of both input control and output status signals, a clock frequency, and an output data character. These signals are listed in Table 5-8.

The format selection logic is basically the same as that used for the transmitter control, and is described in Table 5-7.

The input logic of the transmitter is described in the following paragraphs.

Regardless of the device used, the serial input from the device is loaded into the DL11-W one bit at a time, beginning with the START bit, then the DATA bits (LSB first), the PARITY bit (if used), and the STOP bits.

The bipolar levels of the serial data are applied to pins K (+) and S (-) of the Berg connector. The bipolar level is converted to a TTL level (Drawing DL-5) and fed to pin H. EIA level serial data is received on pin J of the connector and converted to a TTL level which is presented at pin M. Either pin M or pin H is connected to pin E (depending upon type of interface to external device) and becomes the signal TTL SERIAL DATA IN. The serial data is connected to a 2:1 multiplexer which, when the interface is not in the maintenance mode, passes the TTL SERIAL DATA IN signal through to the output, which is then applied to the input (SERIAL IN) of the UART (as shown in Drawing DL-1). The output of the multiplexer is also inverted and fed to a counter used to detect the center of a START bit.

TABLE 5-8

RECEIVER STATUS AND CONTROL LOGIC

Signal Mnemonic	Signal Name	Description
R DONE	Reader Done	The R DONE flag that indicates a full character has been received from the device and is ready for transfer to the Unibus.
P ERR	Parity Error	A status signal indicating that the received character has a parity error. Can be read by the program.
FR ERR	Framing Error	A status signal indicating that the received character has no valid STOP code. Can be read by the program.
OR ERR	Overrun Error	A status signal indicating that the character was not read prior to receiving another character from the device. Can be read by the program.
R CLK	Receiver Clock Pulse	Provides the required receiver clock rate. This rate is 16 times the selected baud rate.
RD7 - RD0	Receiver Data Buffer	Represent the character (five to eight data bits) transferred from the UART to the Unibus after serial-to-parallel conversion.

5.8 UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The Universal Asynchronous Receiver/Transmitter (UART) is an LSI subsystem that accepts binary characters from either a terminal device or a computer, and receives or transmits this character with appended control and error detecting bits. In order to make this subsystem universal, the baud rate, bits per word, parity mode, and number of stop bits are selected by external logic circuits.

The UART is a full duplex receiver/transmitter. The receiver section accepts asynchronous serial binary characters and converts them to a parallel format for transmission to the Unibus. The transmitter section accepts parallel binary characters from the bus and converts them to a serial asynchronous output with start and stop bits added.

All UART characters contain a START bit, five to eight DATA bits, one, one and a half, or two STOP bits, and a PARITY bit which may be odd, even, or turned off. The STOP bits are opposite in polarity to the START bit. This is the maximum format that can be used.

Both the receiver and transmitter are double-buffered. The UART internally synchronizes the START bit with the clock input to ensure a full 16-element (clock periods) START bit independent of the time of data loading. Transmitter distortion (assuming perfect clock input) is less than 3 percent on any bit up to 10 kilobaud. The receiver strobes the input bit with +8 percent of the theoretical center of the bit. The receiver also rejects any START bit that lasts less than one-half of a bit time.

The UART input and output lines are shown on Drawing DL-1. A description of the receiver is given in Paragraph 5.8.1 and a description of the transmitter is given in Paragraph 5.8.2. Note that in the following discussions the mnemonic and pin number of UART input and output lines are given in parentheses.

5.8.1 Receiver Operation

A block diagram of the UART receiver is shown in Figure 5-6. When the receiver is in the idle state, it samples the serial input line (SERIAL IN, pin 20) at the selected clock edges (R CLK, pin 17) after the first mark-to-space transition of the serial input line. If the first sample is a mark (high), the receiver returns to the idle state and is ready to detect another mark-to-space transition. If, however, the first sample is a space (low), then the receiver enters the data entry state.

If the receiver control logic has not been conditioned to the no parity state (a low on pin 35), then the receiver checks the parity of the data bits plus the parity bit following the data bits and compares it with the parity sense on the parity select line (pin 34). If the parity sense of the received character differs from the parity of the UART control logic, then the receiver parity error line (P ERR, pin 13) goes high and causes the P ERR bit in the RBUF register to set.

If the receiver control logic has been conditioned to the no parity state (a high on pin 35), then the receiver takes no action with respect to parity and maintains the parity error line (P ERR, pin 13) in the false (low) state. When the control logic senses a parity error, it generates a P ERR signal. The DATA AVAILABLE signal updates the parity error indicator. Note that the P ERR output is always produced by the UART but is coupled to the RBUF only on DL11-C, D, and E options.

The receiver samples the first STOP bit, which occurs either after the PARITY bit or after the data bits (if no parity is selected). If a valid (high) STOP bit exists, no further action is taken. If, however, the STOP bit is false (low), indicating an invalid STOP code, then the UART control logic provides a framing error indication (a high on FR ERR, pin 13). The status of the framing error bit can also be read from the RBUF if enabled.

Because the serial input from the external device is shifted into the UART a bit at a time (SERIAL IN, pin 20), occurrence of a STOP code indicates that the entire data character has been received and shifted into the receiver shift register. After the STOP bit has been sampled, the receiver control logic parallel transfers the contents of the shift register into the receiver data holding register and then sets the data available (R DONE) flag.

The data available signal also functions as the clock input to the FRAME ERR, PARITY, and OVERRUN flip-flops in the UART status register. At this point, the DA flip-flop is set, the OVERRUN flip-flop is clear but has a high on the data input because of the output from the DA flip-flop, and the PARITY and FRAME ERR flip-flops are set or cleared depending on the signal (true or false) strobed in from the control logic.

An OVERRUN condition indicates that another data character is being sent to the UART before the previous character has been transferred to the DL11-W receiver buffer register. If the DA flip-flop is set, indicating that a character is stored in the holding register, and the UART control logic attempts to set the DA flip-flop again (indicating that a new character has been shifted into the shift register), the DA signal from the control logic provides a clock input to the OVERRUN flip-flop. This flip-flop then sets because the data input is high (DA flip-flop was already set by the previous DA signal).

During normal operation (no OVERRUN condition), the character in the receiver data holding register is strobed onto the Unibus by a read of RBUF which produces SEL 2 L. This signal is applied to the UART reset data available line (pin 18) to clear the flip-flop.

Whenever the serial input line goes from a mark (high) to a space (low) and remains at the low level, the receiver shifts in one character, which is all spaces, then sets the FR ERR indicator and waits until the input line goes high (marking) before shifting in another character.

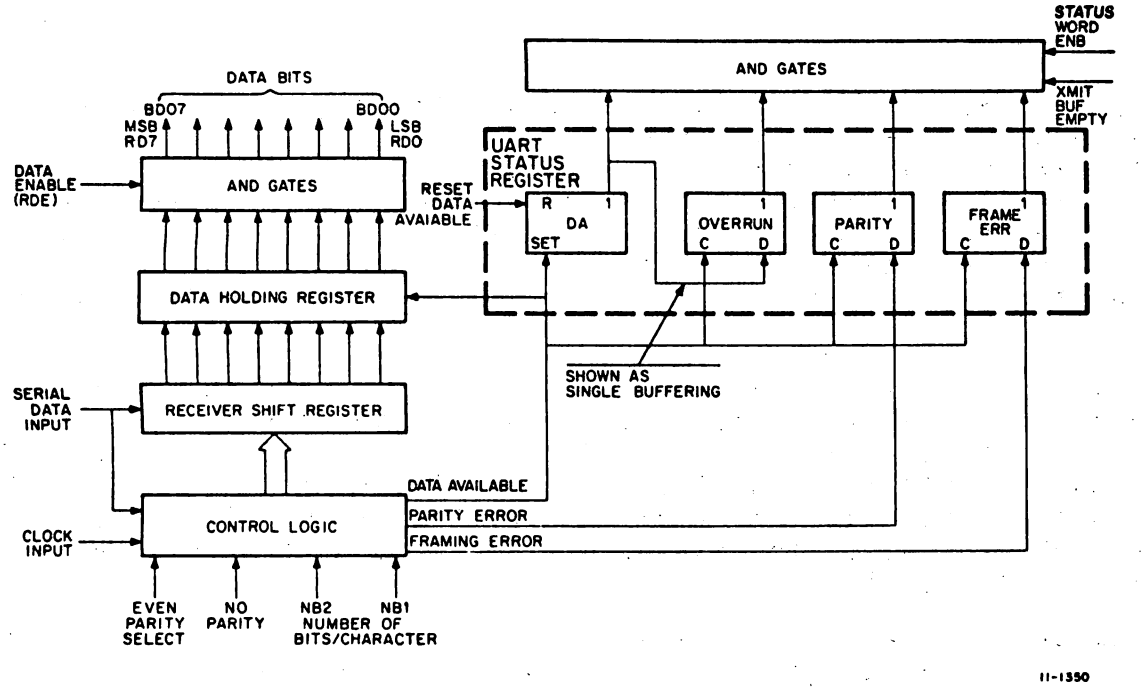


Figure 5-6 UART Receiver - Block Diagram

5.8.2 Transmitter Operation

A block diagram of the UART transmitter is shown in Figure 5-7. When the UART transmitter is in the idle state, the serial output line (pin 25) is a mark (high). When it is desired to transmit data, a parallel character is placed on bus data lines BUS D00 through D07 and strobed into the UART transmitter data buffer (lines connected to pins 26 - 33) by means of the data strobe signal (pin 23). The time between the low-to-high transition of data strobe and the corresponding mark-to-space transition of the serial output line is within one clock cycle (1/16 of a bit time) if the transmitter has been idle. The data strobe signal is LD XD DEL L which is used to load a character from the Unibus into the transmitter buffer register (XBUF).

When the data has been loaded into the UART data buffer, it is next transferred to the transmitter shift register under control of signals from an encoder which selects the format determined by the control logic. This permits selection of parity or no parity (pin 35), the type of parity (pin 39), the number of STOP bits (pin 36), and the number of data bits per character (pins 37 and 38).

The transmitter logic converts the parallel character from the Unibus into a serial output that is in a format selected by the control logic.

The clock input to the timing generator (pin 40) is derived from the DL11-W baud rate circuits (Paragraph 5.9). The other input to the timing generator is the end-of-character (pin 24) signal from the output logic. This line goes high each time a full character (including STOP bits) is transmitted. If this line goes low, it prevents the timing generator from loading another character into the

shift register. The line is normally high when data is not being transmitted and goes low at the start of transmission of the next character.

Whenever the transmitter data buffer is loaded while the previous character is being shifted through to the output line, the START bit of the new character immediately follows the last STOP bit of the previous character.

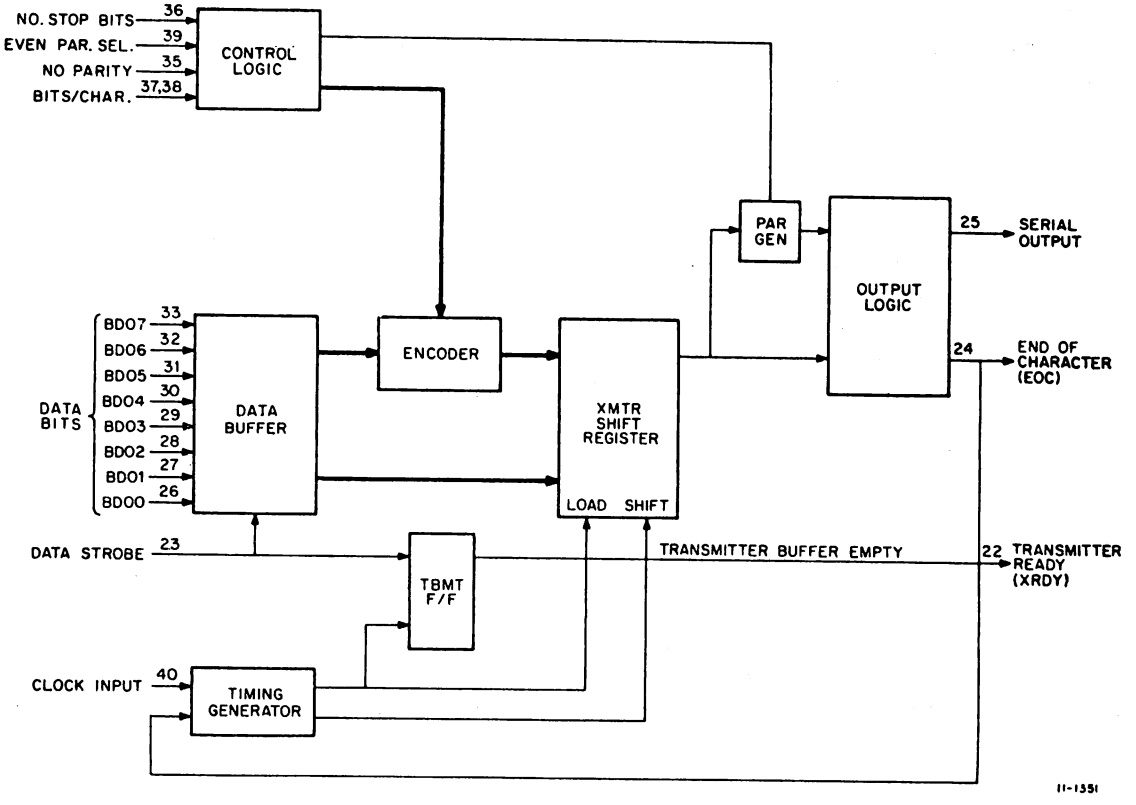


Figure 5-7 UART Transmitter - Block Diagram

When the data strobe (pin 23) signal loads the UART data buffer, the DL11 transmitter buffer (XBUF) is unloaded. Therefore, the data strobe signal sets the TBMT (transmitter buffer empty) flip-flop to provide a signal that becomes XRDY (transmitter ready). This XRDY signal can be read by the program and indicates that a new character can be loaded in the DL11 transmitter buffer.

5.9 BAUD RATE LOGIC

The baud rate logic provides the clock frequencies and, therefore, the baud rates for both the receiver and transmitter sections of the DL11-W interface. The switch-selectable baud rates on the DL11-W are all generated by a single crystal-controlled oscillator applied to two frequency divider circuits. Since all eight different baud rates are simultaneously generated, any one of the eight baud rates may be selected for the receiver and transmitter sections.

Note that the frequencies required by the UART are 16 times the desired baud rates.

The master oscillator operates at a frequency of 5.0688MHz (Drawing DL-6). The master oscillator output is then applied to two divider circuits. One circuit divides the master clock frequency by 2,112 (11,12,16) to produce a frequency of 2.4KHz, which provides a baud rate of 150 (16*150 = 2400). Multiples of 150 (300, 600, 1200, 2400, 4800, 9600) are also produced up to 9600 baud (153.6KHz). The other divider circuit divides the master clock frequency by 2,880 (12,15,16) to produce a freqeuncy of 1.76KHz, which corresponds to a baud rate of 110 (110.16 = 1,760).

The eight different baud rates are applied to two 8:1 multiplexers, one for the receiver clock and one for the transmitter clock.

Each of the multiplexers is controlled by three switches so that the RCVR CLK signal and XMIT CLK signal can be independently controlled. The switch settings for the various baud rate selections is shown in Table 5-9.

TABLE 3.3

BAUD RATE SWITCH SELECTIONS

BAUD RATE	RECEIVER			TRANSMITTER		
	S3-2	S3-3	S3-5	S4-10	S3-1	S3-4
110	OFF	OFF	OFF	ON	ON	ON
150	ON	OFF	OFF	OFF	ON	ON
300	OFF	ON	ON	ON	OFF	OFF
600	OFF	ON	OFF	ON	OFF	ON
1200	OFF	OFF	ON	ON	ON	OFF
2400	ON	ON	ON	OFF	OFF	OFF
4800	ON	ON	OFF	OFF	OFF	ON
9600	ON	OFF	ON	OFF	ON	OFF

5.10 MAINTENANCE MODE LOGIC

The maintenance mode is used to check operation of the DL11-W control logic. Figure 5-8 is a simplified diagram of both the normal and maintenance modes. During normal operation, data from the bus is converted by the transmitter and sent to the external device, or data from the external device is converted by the receiver and sent to the bus.

During the maintenance mode, a character is loaded into the transmitter buffer (XBUF) from the Unibus. This parallel character is then converted to a serial output by the UART transmitter section. However, in addition to entering the external device, the serial data is also fed back into the receiver, which converts it back to parallel data and places it on the bus. If the character received by the bus is identical to the character sent out on the bus, then both the transmitter and the receiver are functioning properly.

Before the maintenance loop can be used, the transmitter must be selected for use and the transmitter buffer (XBUF) loaded with a character. The program selects the maintenance mode by setting bit 02 (MAINT bit) in the transmitter status register (XCSR). This sets the MAINT flip-flop in the transmitter logic (Drawing DL-1).

The MAINT (1) H output of the flip-flop is used as an enabling level for a 4-line-to-1-line multiplexer (IC 74157 on Drawing DL-1). A simplified version of this multiplexer is shown in Figure 5-9. Normally, the gates shown enabled by the MAINT (1) H signal in the figure are inhibited and the serial output from the transmitter, as well as the clock signals, are fed to the logic used during the normal operating mode. However, when MAINT (1) H is present, the gates are qualified and perform two basic functions.

The first function is to gate the serial output of the transmitter (SERIAL OUT H) to the serial input line (SERIAL IN) of the receiver. The second function is to force the RCVR CLK pulse to be the same as the XMIT CLK, regardless of the switch position of the RCVR CLK. When MAINT (1) H is present, the gate receiving RCVR CLK H is inhibited and the XMIT CLK H pulse is gated through to the RCLK H line of the receiver. Although not shown in the figure, the XMIT CLK H is also applied to the clock line of the transmitter.

Because the receiver logic is activated by a START bit (regardless of where the START bit comes from), the receiver is activated as soon as it receives the first input from the transmitter. After the receiver assembles the data, the program can compare the received character with the transmitted character to determine if the DL11-W interface is functioning properly.

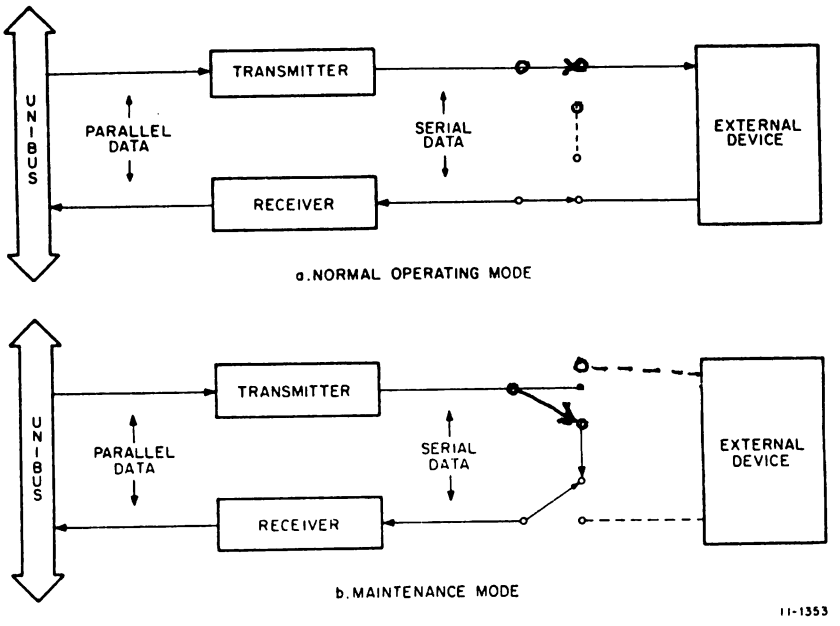


Figure 5-8 Operating Modes

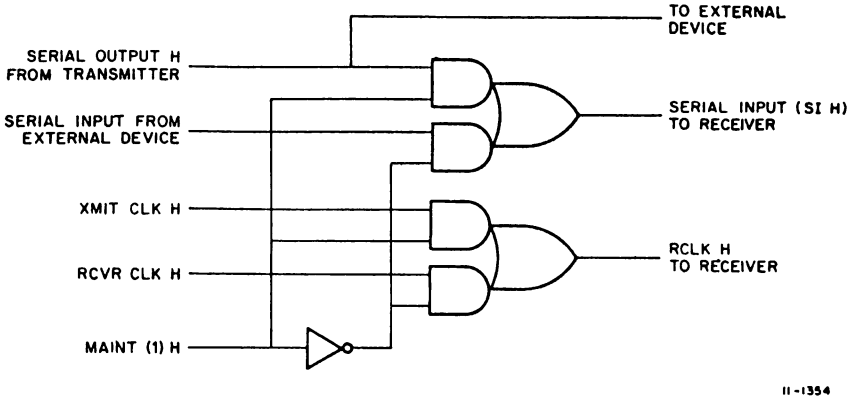


Figure 5-9 Maintenance Logic - Simplified Diagram

5.11 20MA CURRENT LOOP LOGIC

20MA current loop circuits are provided for the serial data transmitter and receiver and for the paper-tape reader control. Two modes of operation are available for the 20MA current loop circuits; active and passive. In active mode, the DL11-W is the source of the 20MA of current which is switched on or off depending upon the level of the SERIAL OUT line. In passive mode, the current loop circuit switches, on or off, current which is sourced by the external device. Figure 5-10 shows a simplified diagram of the receiver and transmitter circuits in active and passive mode. Table 5-10 shows the switch selections for the two modes of operation for each 20MA current loop.

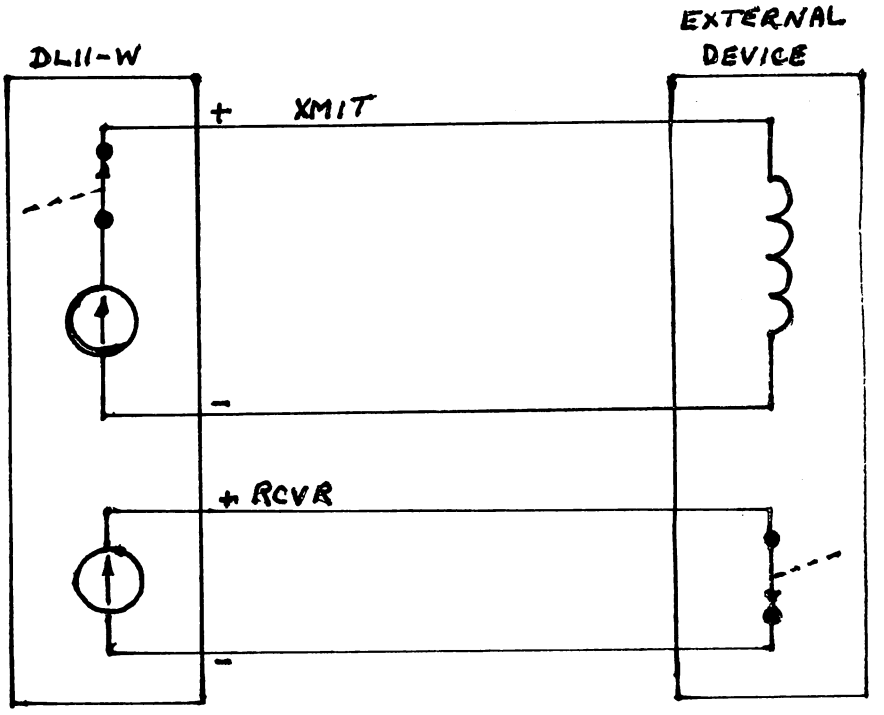


Figure 5-10A DL11-W in Active Mode

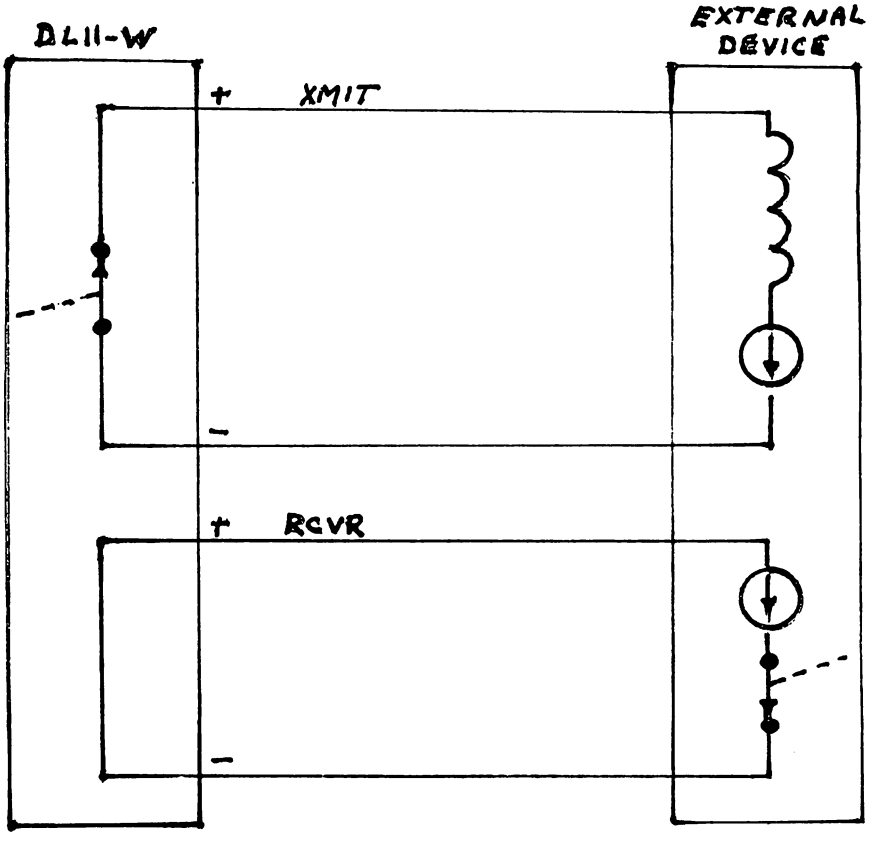


Figure 5-10B DL11-W in Passive Mode

TABLE 5-10

SWITCH SELECTIONS FOR ACTIVE AND PASSIVE MODES

TRANSMITTER	S1-1	S1-2	S1-3	S1-6	S1-7
ACTIVE	ON	ON	OFF	OFF	ON
PASSIVE	OFF	OFF	ON	ON	OFF
RECEIVER	S3-6	S3-7	S3-8	S3-9	S3-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF
READER ENABLE	S1-4	S1-5	S1-8	S1-9	S1-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF

5.12 EIA LEVEL CONVERTER LOGIC

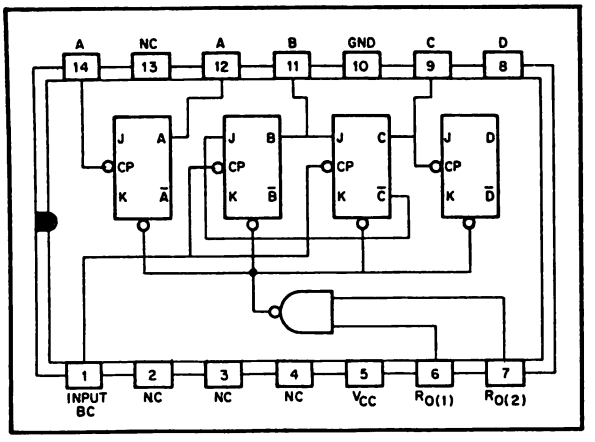
Bipolar EIA level converters are provided for serial data out and serial data in interfacing. Serial output data, SERIAL OUT H, is applied to an EIA level converter and the output, which is a bipolar signal (approximately ±10V), is available at pin F on the Berg connector. Bipolar EIA level input serial data is received at pin J of the Berg connector and converted to a TTL level signal, which is then available at pin M on the Berg connector. If EIA level interfacing is being used, pin M must be connected to pin E of the Berg connector; this is normally done by the connector on the cable used to interface the DL11-W and the external device.

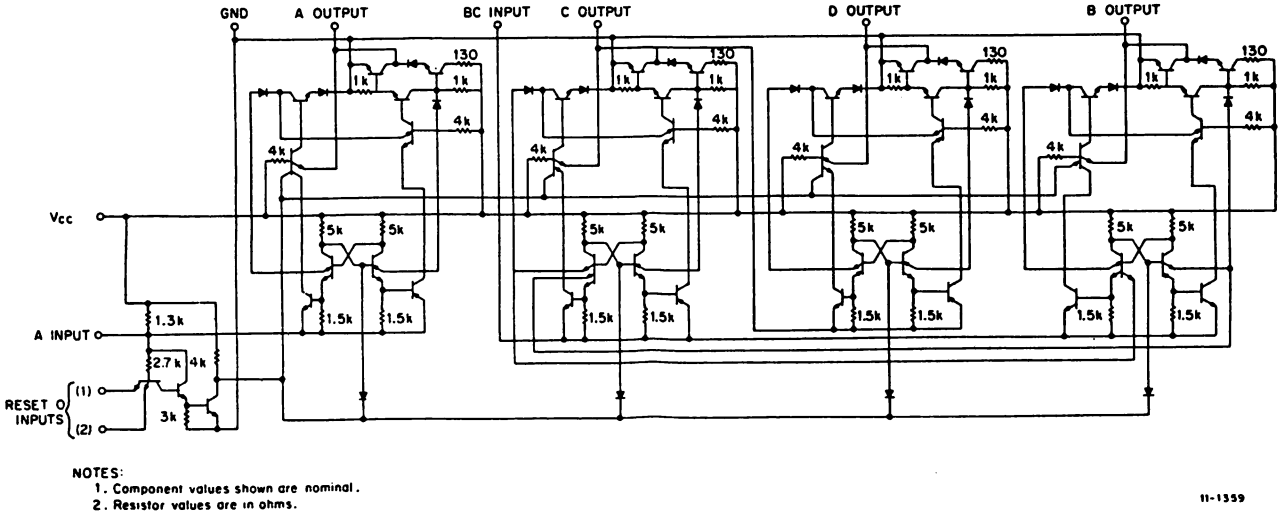
The signals DATA TERMINAL READY and RQST TO SEND are permanently strapped on (high) and are available at pins DD and V of the Berg connector, respectively.

APPENDIX A

IC SCHEMATICS

Appendix A contains schematics of some of the integrated circuit chips used on the DL11-W.





NOTES:
1. Component values shown are nominal.
2. Resistor values are in ohms.

11-1359

Figure A-1 7492 FREQUENCY DIVIDER

7493 FREQUENCY DIVIDER

TOGGLE INPUT PULSE	OUTPUT			
	Y1	Y2	Y3	Y4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

*TRUTH TABLE

*Applies When 7493 Is Used As 4-Bit Ripple-Through Counter.

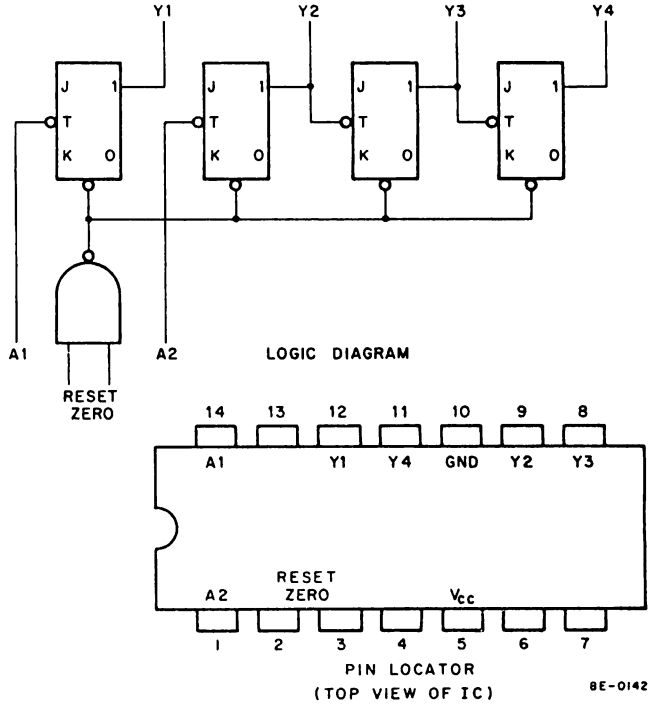
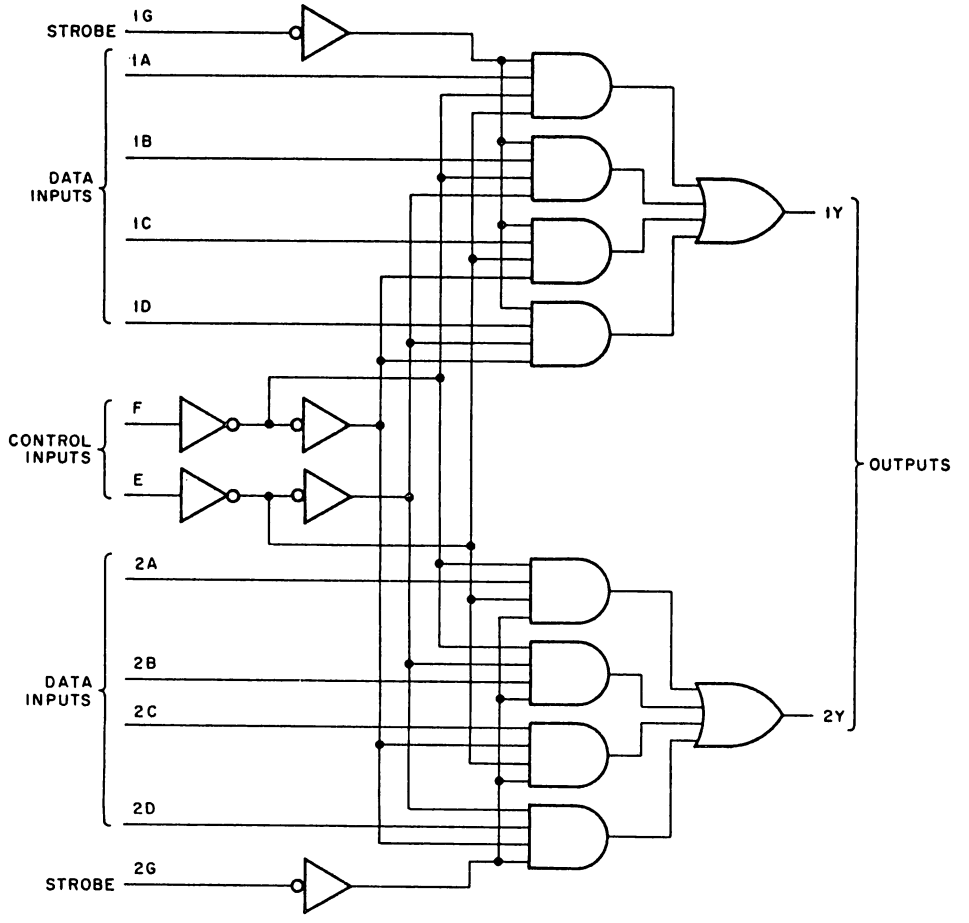


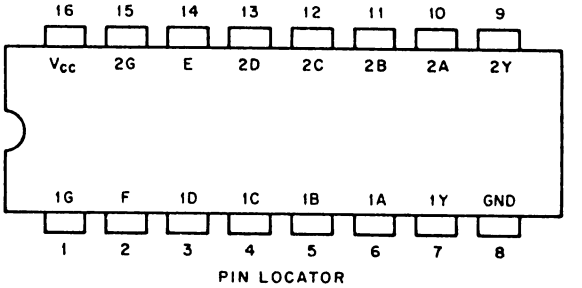
Figure A-2 7493 FREQUENCY DIVIDER



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



PIN LOCATOR
(TOP VIEW OF IC)

8E-0138

Figure A-3 74153 4-LINE-TO-1-LINE MULTIPLEXER

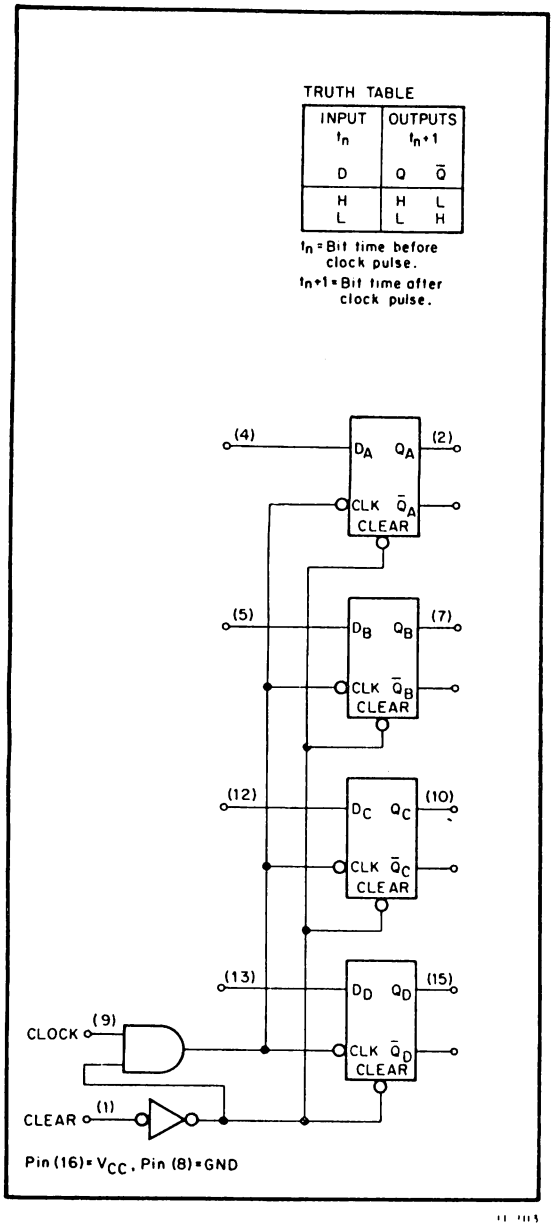


Figure A-4 /4175 QUAD D-TYPE FLIP-FLOP

APPENDIX B

VECTOR ADDRESSING

B.1 INTRODUCTION

Because the DL11-W SLU/RTC option is basically a communications device, interrupt vectors must be assigned according to the floating vector convention used for all communications devices. These vector addresses are assigned in order from 300 to 777 according to a specific method that ranks the type of devices in a particular PDP-11 System.

The first vector address (300) is assigned to the first DC11 Serial Asynchronous Line Interface in the system; the next DC11 (if used) is then assigned vector address 310, etc. The vector addresses are assigned consecutively to each unit of the second-ranked device type (KL11 or DL11-A or DL11-B or DL11-W), then to the third-ranked device (DP11), and so on in accordance with the following list:

1. DC11 Asynchronous Line Interface
2. KL11 Teletype Control (or DL11-A, DL11-B or DL11-W)
3. DP11 Synchronous Serial Modem Interface
4. DM11 Asynchronous Serial Line Multiplexer
5. DN11 Automatic Calling Unit
6. DM11-BB Modem Control
7. DR11-A Device Registers
8. DR11-C General Device Interface
9. DT11 Bus Switch
10. DL11-C Asynchronous Line Interface or DL11-W
11. DL11-D Asynchronous Line Interface or DL11-W
12. DL11-E Asynchronous Line Interface

If any of these devices are not included in a system, the vector address assignments move up to fill the vacancies. If a device is added to an existing system, its vector address must be inserted in the normal position and all other addresses must be moved accordingly. If this procedure is not followed, DEC software cannot test the system.

Note that the floating vectors range from addresses 300 to 777 but

addresses 500 through 534 are reserved for special bus testers. In addition, address 1000 is used for the DS11 Synchronous Serial Line Multiplexer.

An address map is shown in Figure B-1 and a list of the vector addresses is given in Paragraph B.2. It should be noted that the system Teletype (KL11) is not part of the floating vector scheme and is assigned vector addresses 060 and 064. Therefore, if a DL11-W is used as a control for the sytem teletype console, it should be assigned addresses 060 and 064. All other DL11-Ws would follow the floating vector conventions.

B.2 INTERRUPT VECTORS

000	RESERVED
004	ERROR TRAP
010	RESERVED INSTRUCTION TRAP
014	DEBUGGING TRAP
020	IOT TRAP
024	POWER FAIL TRAP
030	EMT TRAP
034	"TRAP" TRAP
040	SYSTEM SOFTWARE COMMUNICATION WORDS
044	SYSTEM SOFTWARE COMMUNICATION WORDS
050	SYSTEM SOFTWARE COMMUNICATION WORDS
054	SYSTEM SOFTWARE COMMUNICATION WORDS
060	TELETYPE IN OR DL11-W CONSOLE INTERFACE
064	TELETYPE OUT OR DL11-W CONSOLE INTERFACE
070	PC11 HIGH-SPEED READER
074	PC11 HIGH-SPEED PUNCH
100	KW11-L LINE CLOCK OR DL11-W LINE CLOCK
104	KW11-P PROGRAMMABLE CLOCK
110	DR11-A (REQUEST A)
114	DR11-A (REQUEST B)
120	XY11 XY PLOTTER
124	DR11-B
130	AD01
134	AFC11
140	AA11-A,B,C,E SCOPE
144	AA11 LIGHT PEN
150	
154	
160	
164	
170	USER RESERVED
174	USER RESERVED
200	LP11 LINE PRINTER CONTROL
204	RF11 DISK CONTROL
210	RC11 DISK CONTROL
214	TC11 DECTAPE CONTROL
220	RK11 DISK CONTROL
224	TM11 MAGTAPE CONTROL

```
230         CR11 CARD READER CONTROL
234         UDC11
240         11/45 PIRQ
244         FPU ERROR
250
254         RP11 DISK PACK CONTROL
260
264
270         USER RESERVED
274         USER RESERVED
300<-FLOATING VECTORS START AT THIS ADDRESS
304
310
314                              Note
320
324         Floating vectors start at address 300 and are
330         assigned in the following order:
334
340
344         all DC11s, then
350         all KL11s,* then
354         all DP11s, then
360         all DM11s, then
364         all DN11s, then
370         all DM11-BBs, then
374         all DR11s, then
400         all DT11s, then
404         all DL11-Cs,** then
410         all DL11-Ds,** then
414         all DL11-Es
420
424
430         * or DL11-As, DL11-Bs, or DL11-W's
434
440         ** or DL11-W's
444
450
454
460
464
470
474
500         SPECIAL BUS TESTERS
504         SPECIAL BUS TESTERS
510         SPECIAL BUS TESTERS
514         SPECIAL BUS TESTERS
520         SPECIAL BUS TESTERS
524         SPECIAL BUS TESTERS
530         SPECIAL BUS TESTERS
534         SPECIAL BUS TESTERS
540
544
550
554
560
```

```
564
570
574
600 through 774nFLOATING VECTORS END HERE
1000nDS11
```

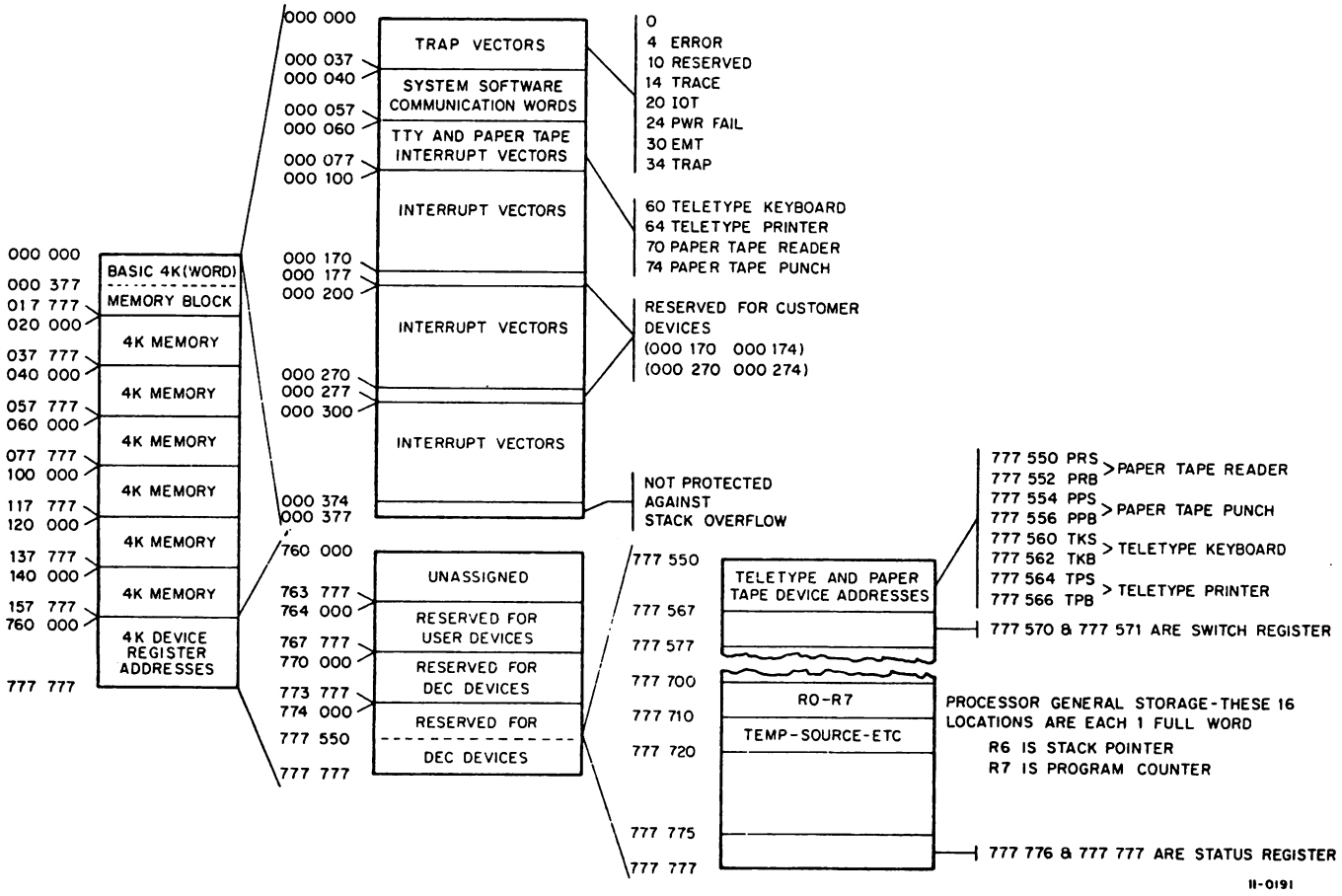


Figure B-1 Address Map