DOCUMATION OM-200 READER

INTRODUCTION

GENERAL

This manual provides operational, interface and maintenance information for the OM 200 Optical Mark Sense Card Reader manufactured by Documation, Incorporated, P. O. Box 1240, Melbourne, Florida 32901. The manual is sectionalized to cover operational instructions, theory of operation, interface details, preventive maintenance, and repair. The appendix includes electrical schematics and wiring details.

The OM 200 Card Reader shown in Figures 1 and 2, is designed to read Mark Sense Cards of ANSI Specification X3.11 1969, for the 12-Row, 80-Column card. The hopper capacity is adequate to hold approximately 550 cards of .007" thickness. These are separated from the stack sequentially and moved past a fiber optics phototransistor read station where the data is recognized in a serial, column-by-column manner. Data columns can be either mark sense or punch columns and can be intermixed on a per card basis. The cards are then stacked into the output hopper in the same order as they were originally put into the reader. The reading cycle is externally controlled for single card selection or continuous run. In the continuous mode, the reader will read 285 cards per minute.

The OM Series card readers are specifically designed for continuous duty operation in adverse operational environments. The chassis is of heavy duty construction and all components have been chosen to provide for rugged, reliable performance. The vacuum-type picker has a remarkable tolerance to mutilated, warped, and edge-damaged cards. The short card track and gentle acceleration forces of the card handling mechanism yield insignificant card wear.

The information contained in this manual is accurate and complete as of the date of publication. Documation will continue to improve bothsits products and the effectiveness of its documentation. Comments and suggestions as to how this manual may be improved are solicited. Address comments to:

Engineering Writer
DOCUMATION INCORPORATED
P. O. Box 1240
Melbourne, Florida 32901
(305) 724-1111

OM 200 SPECIFICATIONS SUMMARY

Reading Speed:	285 cards per minute maximum in continuous run. Single card cycle: 210 milliseconds.
Card Type:	80 Column Mark Sense cards as specified in the Card Specifications Section.
Data Field:	Reads Mark Sense and Punched Columns intermixed on a per card basis.
Control:	Demand feed, one card at a time under external program control. Reader will continuous run as long as the Pick Command remains TRUE.
Hopper Size:	4.0 inches (approximately 550 cards of 7 mil thickness).
STACKER SIZE:	4.0 inches (approximately 550 cards of 7 mil thickness).

Power Requirements:

Voltage:	115 VAC ± 10%, single phase, @ 60 Hz (standard model) 230 VAC ± 10%, single phase, @ 50 Hz (export model)
Power:	950 VA starting load for 3 sec 400 VA running load

Size:

Height:	11 inches	27.9 cm
Width:	19¼ inches	48.9 cm
Depth:	14 inches	35.5 cm
Weight:	60 lbs.	27.3 kg

CARD SPECIFICATIONS

Card Design

Because the Mark Sense card's image field is determined and tailored by the customer to meet a particular application, the following is presented to aid in the design of a Mark Sense Data Card.

The shaded portions of Figure 3 show the areas in which data and clock marks can be placed.

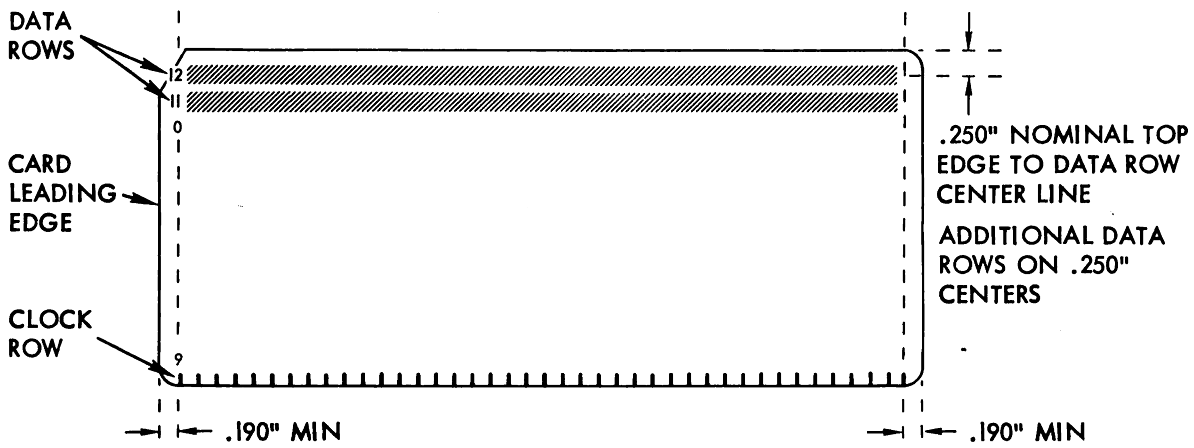


Figure 3. Marking Areas

Data columns are constructed by a clock mark immediately preceding the data column, the data column area and then another clock mark. Figure 4 shows a typical data column and the read area for each data row.

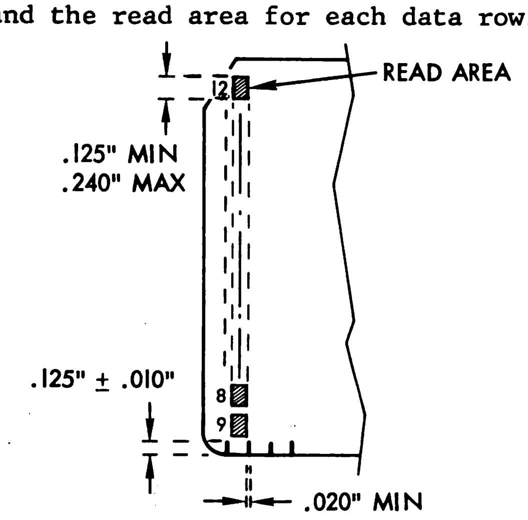


Figure 4. Data Column

Any pencil mark or punched hole meeting the data specification and lying in the shaded area between the clock marks will be read as data.

A marking constraint with mark identifier is normally used to place and identify a data mark in the data field. Figure 5 depicts a typical marking constraint.

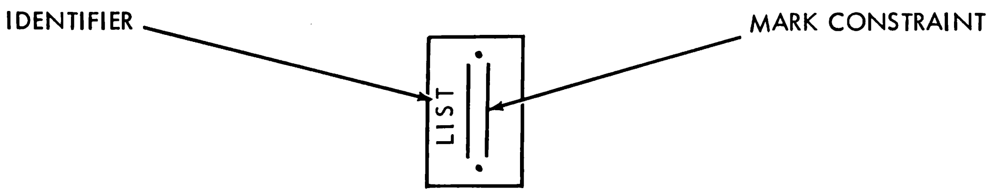
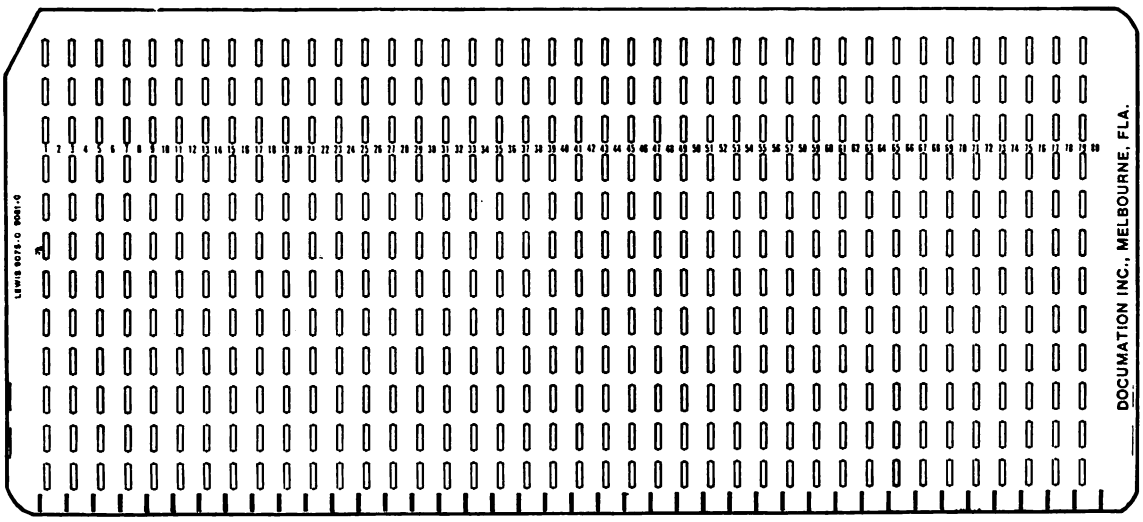


Figure 5. Mark Constraint

To indicate a list a vertical pencil mark would be placed within the constraint.

An example of a general purpose, 40 column Mark Sense Card is shown in Figure 6. This card was designed by Documation Incorporated.



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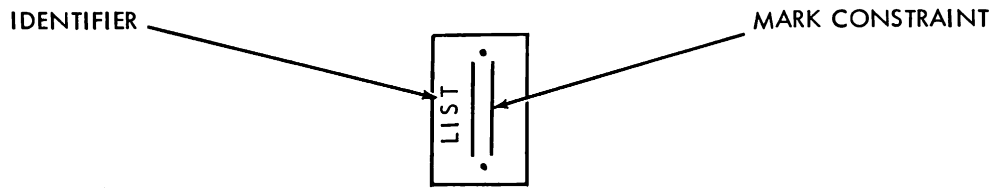

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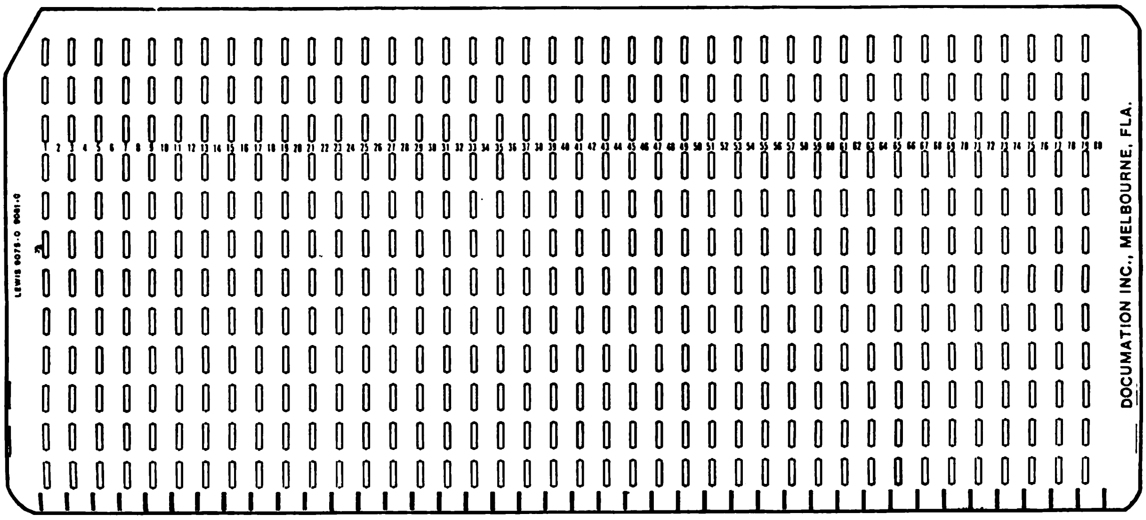

Figure 6. Mark Sense Card

A few important points to consider when designing a Mark Sense Card are:

1) A clock mark should never lie on a vertical line with a data constraint, i.e., data is only read between clock marks.

2) Spacing between clock marks should be no more than .5 inches.

3) Registration from card leading edge to data is important only when punch columns are being set up, i.e., punch columns will be registered by the punch.

4) All data constraints and identifiers must be printed in reflective ink.

Card Stock

A card will be acceptable for use as a Mark Sense Card provided:

1) The card meets American National Standard's specification ANSI X3.11-1969, Specification for General Purpose Paper Cards for Information Processing.

2) The average reflectance* of the card does not fall below 80 percent.

3) Blemishes and printing in the marking field of the card reflect at least 85 percent of the average reflectance of that particular card. (Therefore, a card whose average reflectance is 90 percent may not have a blemish or printing that indicates less than 0.85 x 0.90, or 76.5 percent.)

4) The card does not contain any non-reflective printing or handwriting anywhere to the left of Column 1 except in a vertical band 1/32 of an inch wide along the left edge of the card.

NOTE: White and natural cards manufactured to card industry standards are usually satisfactory. Only those marks described in the Data Section will be permitted on the card surface.

Data Constraints and Identifiers

All Data Constraints and Identifiers must be printed in reflective ink. Reflectance of constraints and identifiers must not fall below 85% of the average background reflectance.

* Reflectance measurements taken using a Macbeth Standard Reflectance plaque as a calibration standard.

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DATA

Mark Sense Data

A mark must be a vertical line using a #2 pencil or equivalent marking material.

The minimum dimensions are: width, .015"; length, .125 centered within data row area.

The maximum dimensions are: width, from trailing edge of previous clock mark to leading edge of next clock mark; length, .240" centered within data row area.

The mark must have an average reflectance that is less than or equal to 28% of the reflectance of that portion of the card immediately adjacent to the mark. Single stroke marks with a #2 pencil will meet this specification.

An erasure must have an average reflectance that is greater than or equal to 75% of the reflectance of the portion of the card immediately adjacent to the erasure.

PUNCH DATA

Punch data must meet American National Standard ANSI X3.21-1967 specifications.

Clock Marks will be as specified in Figure 7. All Clock Marks must be printed in non-reflective ink. Marks will have an average reflectance of less than or equal to 28% of the reflectance of the portion of the card immediately adjacent to the clock mark.

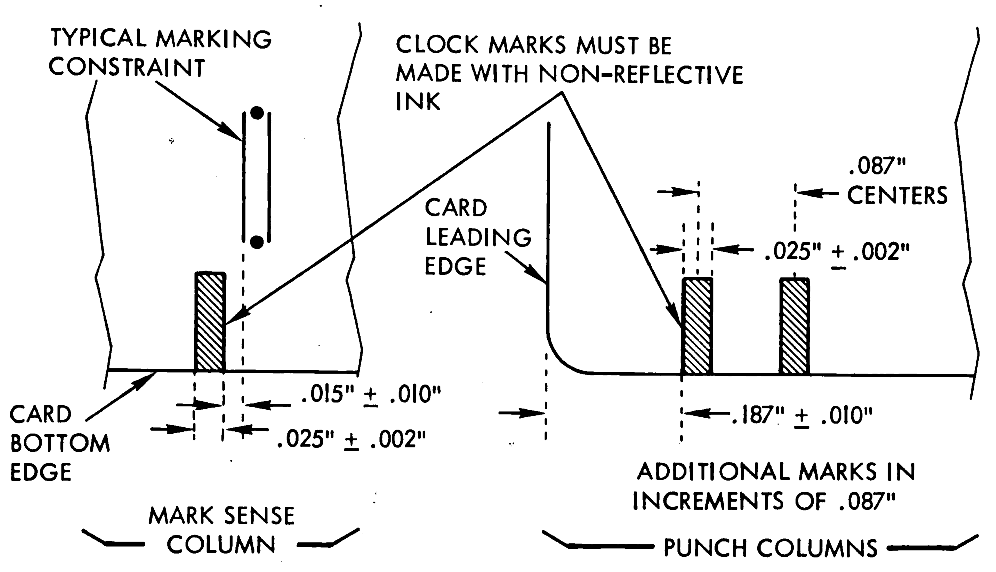

Figure 7. Clock Marks

- 7 -

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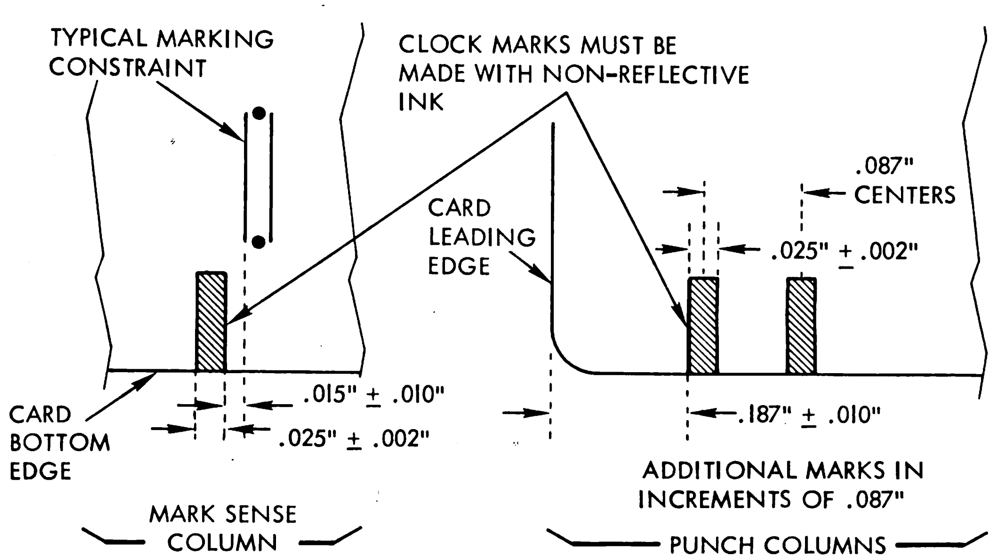


Figure 7. Clock Marks

Figure 7 gives Clock Mark specifications for mark and punch columns. Note that punch column clock marks are registered with respect to the leading edge of the card while mark column clock marks are registered with respect to the mark column.

Clock marks must be used for all columns for which an index mark is required. An additional clock mark is also required in column zero to initialize the data circuits to the card's surface.

THEORY OF OPERATION / ENG. DRAWINGS
DOCUMENTATION OM-200

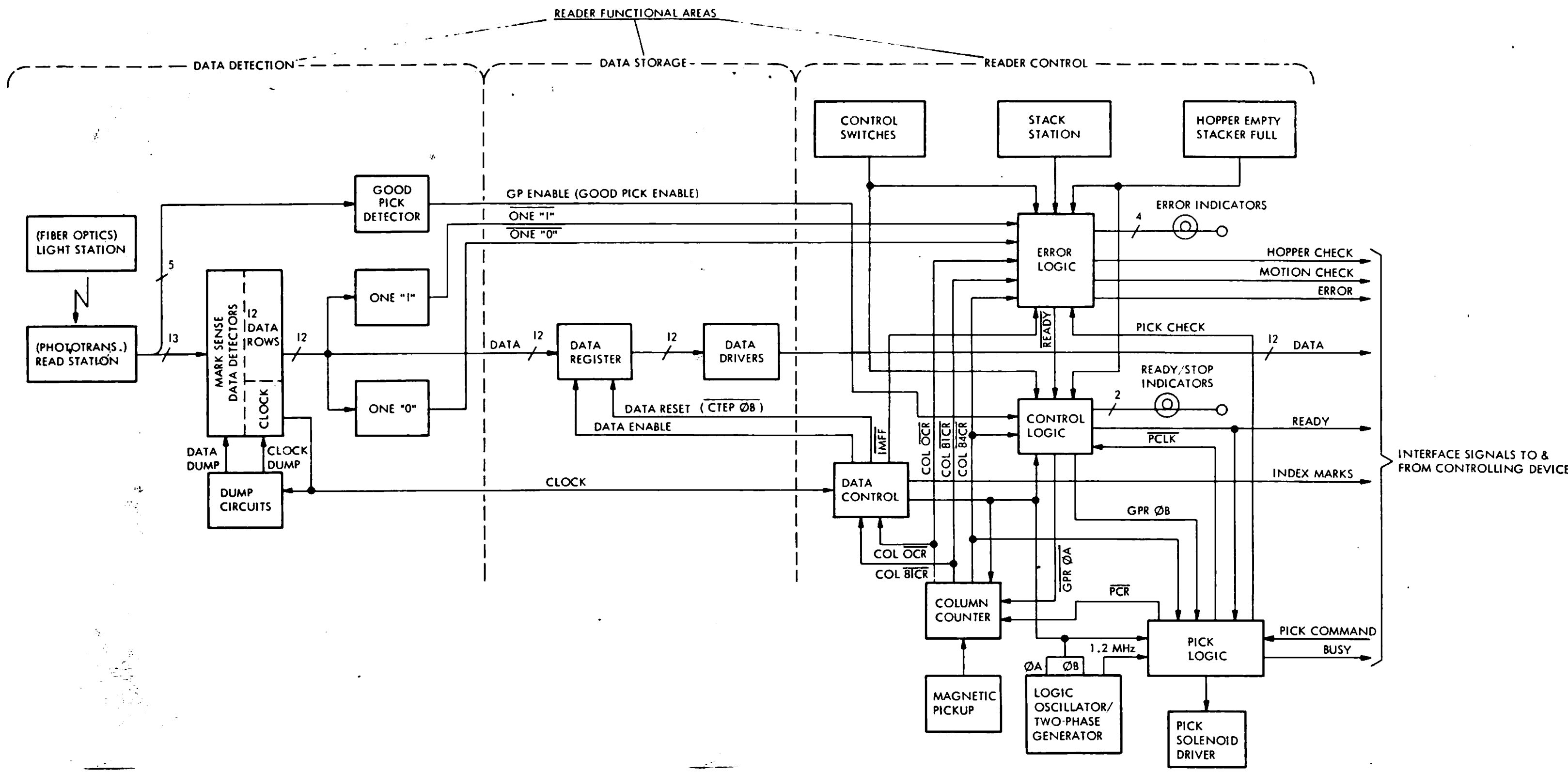


Figure 10. Block Diagram - OM Series Card Reader

THEORY OF OPERATION

CARD TRACK

The Documation card reader line is unique in several respects, in that card wear is insignificant and a card jam is virtually an impossibility. The card track is designed around a patented vacuum picker which works in conjunction with riffle air in the input hopper to produce a card reader which is very tolerant to damaged cards. This tolerance extends to cards which have been badly worn, edge nicked, warped, bent, folded or otherwise damaged as a result of rough handling.

The riffle air acts on the first half inch of cards in the input hopper so that they stand apart, individually "air cushioned" from the rest of the card deck and each other. This prevents the cards from sticking together in case of static electricity, hole locking, or torn webs. Should the cards have been subjected to high humidity conditions prior to being loaded into the card reader, the riffle air also minimizes the effect of swelling or frictional increases between the cards.

The picker mechanism utilizes a strong vacuum to grasp the bottom card, and upon command, draw it away from the bottom of the stack. The card is smoothly accelerated through the wide throat into the constant speed drive rollers. The design of the vacuum picker and its associated throat block prevent the unit from double picking so well that cards which are even stapled together will not enter the card track. Should cards which are stapled or taped together be inadvertently put in the input hopper, the card reader will stop, indicating a PICK CHECK. The operator can remove the staples, separate the cards, re-enter them in their proper position in the deck and resume reading.

The card track itself is very short so that at no time is more than one card in motion. The combination of damaged card tolerance, gentle card treatment and short card track have produced a card reader which is virtually jam proof. Card life has proven to be in excess of 1000 passes.

DATA RECOVERY

The logic block diagram for the OM Series Card Reader is shown in Figure 10. The description that follows applies to all Documation OM Series Card Readers since the reliable recovery of data from cards passing down the card track is accomplished in the same manner regardless of track velocity.

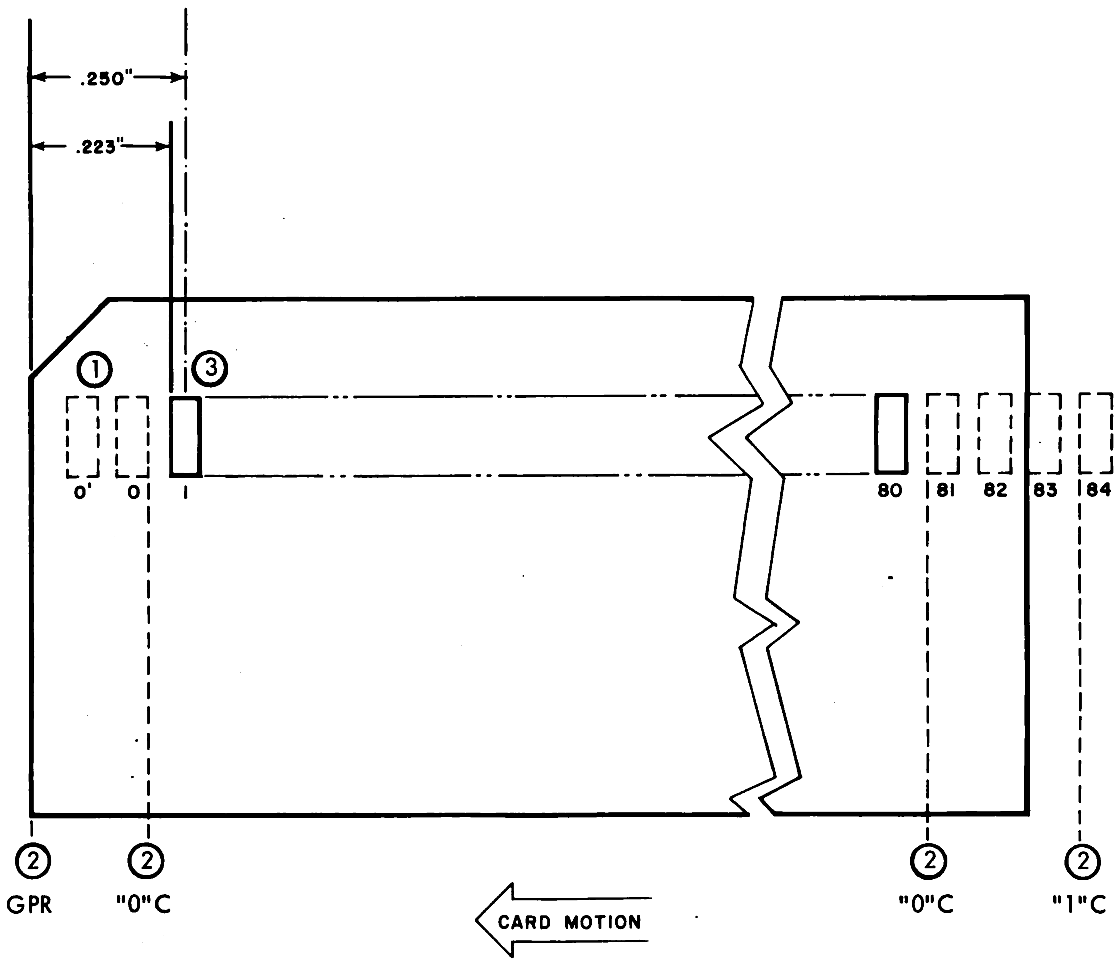
Data recovery is accomplished by the functions of Reader Control, Data Detection and Data Storage. Reader Control synchronizes the electronic scanning of the card with the mechanical actions of the reader. This involves card picking, card movement through the read station, data flow control and card stacking. Data Detection converts the reflections from card surface into usable digital signals for Data Storage. Data storage provides the data buffering and retainment required for data transfer from the reader.

Reader Control

Primary control timing is established by the 1.2 MHz Logic Oscillator and the Two-Phase Generator. These are used to shift, store and control other logic operations. Card movement speed is established by the hysteresis synchronous drive motor, belts and steel drive rollers. Electronic tracking of card movement is accomplished by a timing disk consisting of a ferrous notched wheel mounted to one of the steel drive roller shafts. A magnetic reluctance pickup is used with the timing disk to provide the synchronization signals to the reader electronics.

When a PICK COMMAND is received from the controlling device, card processing will be started provided no alarm conditions exist. The Pick Logic then produces a PICK signal to the Solenoid Driver, a $\overline{\text{PCLK}}$ signal to the Control Logic, and a pick-command reset ($\overline{\text{PCR}}$) to the Column Counter. These actions initialize the various control circuits and energize the solenoid to pick a card from the input hopper. If a card does not reach the read station, the PICK CHECK alarm is raised.

The Read Station and Stack Station utilize phototransistor sensors to both read the card's mark or hole pattern and to monitor the card's movement. When a card is picked and moved into the card track, the leading edge is detected by a phototransistor in the Read Station. This produces a GOOD PICK ENABLE that activates the Column Counter. The Column Counter then counts Magnetic Pick Up Pulses from the timing wheel as the card moves past the Read Station, synchronizing the mechanical card movement with the electronic circuits. The Column Counter generates an all zeros check at column 0 and 81 and an all ones check at column 84. Figure 11, Timing Relationship for Standard Card, shows these check positions. These checks provide a quality check on both the Mark Sense Data Detectors and the mechanical card movement.



NOTES

① DASHED LINES INDICATE PSEUDO DATA POSITIONS ON CARD.

② "0"C = ALL ZEROS CHECK

"1"C = ALL ONES CHECK

GPR = GOOD PICK RESET

③ HOLE SIZE EXAGGERATED FOR EXPLANATION.

Figure 11. Timing Relationship for Standard Card

Data Detection

Following GOOD PICK ENABLE, the Mark Sense Data Detectors scan the card for pencil marks or punched holes as it passes through the Read Station. Twelve of the Mark Sense Data Detectors scan the 12 data rows and the 13th Mark Sense Data Detector scans the clock channel for clock marks. Since data is recognized only between clock marks, physical registration from the card leading or trailing edge for data columns is irrelevant and no synchronization between mechanical card movement and data columns is required.

Each Mark Sense Data Detector tracks the card's surface reflectivity. A fiber optics Light Station provides a narrow band of light incident upon the card surface for each of the detectors. This light is then reflected from the card's surface through a fiber optics bundle to the Read Station phototransistors. Since the card's surface reflectivity determines the amount of light reflected to the phototransistor, the phototransistor's output is an electronic representation of the card's surface reflectivity. The outputs of the 13 phototransistors are converted from these reflectivity representations to digital signals by the Mark Sense Data Detectors for Data Storage.

Data Storage

Pencil marks and punched holes recognized by the Mark Sense Data Detectors are transferred in column form to the Data Register. Timing for data storage is derived from the card clock marks. The leading edge of each clock mark begins a period of no data storage allowing data to be transferred from the reader. The trailing edge of each clock mark is used to reset the Storage Register and enable a new period of data transfer from the Mark Sense Data Detectors to the Data Register. Data storage includes Data Drivers that provide buffering between the Data Register and the interface lines.

DETAIL OPERATIONAL DESCRIPTION

The following gives a detailed description of each block shown in Figure 10, Block Diagram - OM Series Card Reader. The descriptions are designed to give the reader an in-depth understanding of how the card reader works without the usual logic gate-by-gate description.

The reader should familiarize himself with the signal mnemonics used in the text description and contained in Appendix C since it will aid in interpreting both the description that follows and the detailed logic schematics of Appendix A.

Reader Control

The following is a detailed description of each block shown under Reader Control in Figure 10 - Block Diagram - OM Series Card Reader.

Logic Oscillator/Two-Phase Generator

The block diagram and timing diagram for the Logic Oscillator/Two-Phase Generator is shown in Figure 12. The Logic Oscillator is two monostable multivibrators (MSMVs) connected in a closed loop and oscillating at 1.2 MHz ± 2.5%. The MSMVs used are very stable over a wide range of temperatures and voltages with cumulative change due to temperature and voltage over the reader's specified range of ± .5% or less. The oscillator runs at a frequency determined by two precision RC networks whenever reader power is applied. To ensure oscillation the Restart Logic Monitors the output of each MSMV and as long as one of the MSMVs is active the Restart Logic is held off. If at any time one of the oscillator's MSMVs does not fire, the Restart Logic will begin oscillation within 5 us providing triggering inputs to the MSMV oscillator.

The Two-Phase Generator divides the 1.2 MHz oscillator's output by two and alternately directs the negative going portion of the 1.2 MHz to ØA or ØB. Reference timing waveforms of Figure 12.

The 1.2 MHz, ØA and ØB signals are used throughout the reader as a timing source.

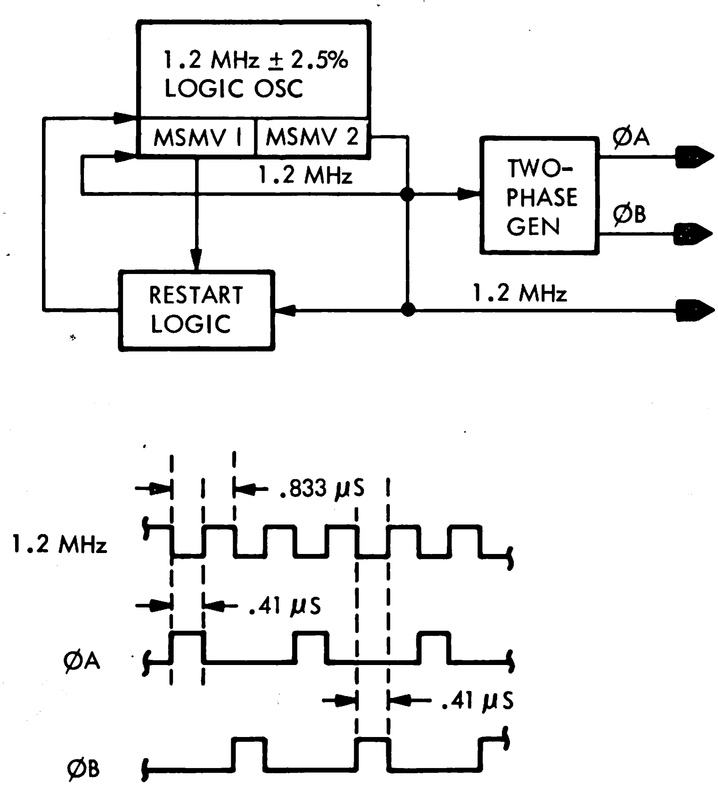


Figure 12. Logic Oscillator/ Two-Phase Generator

Control Logic

The Control Logic (Figure 13) contains the Ready/Stop Logic, Power On Reset, Blower Control, Reset Control and Good Pick Generator.

At reader power turn on, a three-second $\overline{\text{POR}}$ is initiated. See timing of Figure 13. $\overline{\text{POR}}$ OR'ed with $\overline{\text{RESET}}$ to form $\overline{\text{POR + RESET}}$ resets all control circuits within the reader and initializes the reader for operation. The long $\overline{\text{POR}}$ of three seconds allows the blower to come up to speed before the controlling device or an operator can initiate a reader operation. The reader is now brought to the ready state by the operator depressing and releasing the RESET switch. Note that while the RESET switch is depressed $\overline{\text{POR + RESET}}$ again goes low providing a reset to all reader control logic. The Reset Control is designed to ignore all RESET switch signals while a read cycle is in progress. Signals $\overline{\text{PCLK}}$ and $\overline{\text{84CR}}$ or $\overline{\text{CR}}$ identify the beginning and end of a read cycle.

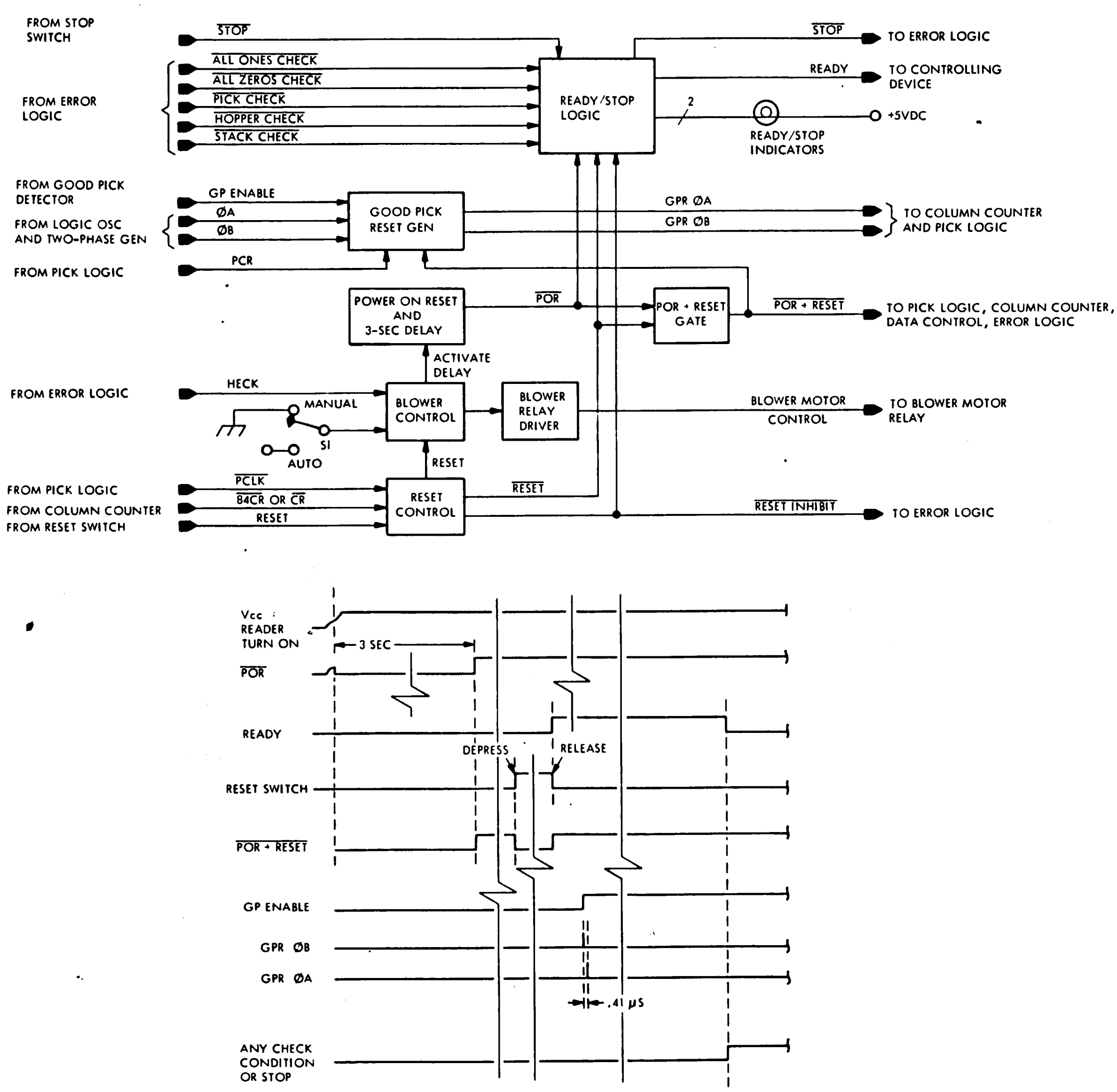


Figure 13. Control Logic Diagram and Timing

Reader READY is signalled to the controlling device by the Ready/Stop Logic when the Reset Switch is released provided HOPPER CHECK is not being presented by the Error Logic. (All other Error Logic Check signals will be reset by POR and RESET.) Reader READY is indicated to the operator by the Reset Switch lighting green. The controlling device can now begin a read cycle by transmitting a PICK COMMAND to the reader. READY will be reset upon receipt of any CHECK signal from the Error Logic or if the Stop switch is depressed by the operator and RESET INHIBIT is not present. The Ready/Stop Logic gates the STOP signal with RESET INHIBIT preventing READY from being reset due to STOP during a card read cycle. RESET INHIBIT, generated by the Reset Control, is set by PCLK and reset by 84 CR or CR. The Stop Condition is indicated by the Stop Switch lighting red.

During a card read cycle, the Good Pick Reset Generator will detect a G P ENABLE and process this signal with the clock phases ØA and ØB to produce GPR ØB followed in .41 microseconds by GPR ØA. These signals are used to start the Column Counter and reset the Pick Logic.

The Blower Control provides signals to control AC power to the reader's blower motor. The blower motor automatically shuts down when a HECK (Hopper Empty Check) condition exists and switch S1 is in the Auto position. After the HECK condition is corrected by reloading the input hopper, depressing of the Reset Switch will cause the Blower Control logic to activate the three-second POR. The three-second POR provides sufficient time for the blower to reach operating speed before a reader operation can begin. When the Auto/Manual switch is in the Manual position, the blower remains on as long as ready power is applied.

Pick Control

Once the reader is brought to ready condition, a PICK CMD from the controlling device can be accepted by the Pick Control. (Figure 14, see diagram and timing.)

The Pick Logic will then:

1. Generate the PCLK.
2. Initiate a PICK pulse that drives the picker solenoid.
3. Control the PICK pulse length.
4. Wait out the interval while the card leading edge is accelerated to the read station (14 to 27 ms).

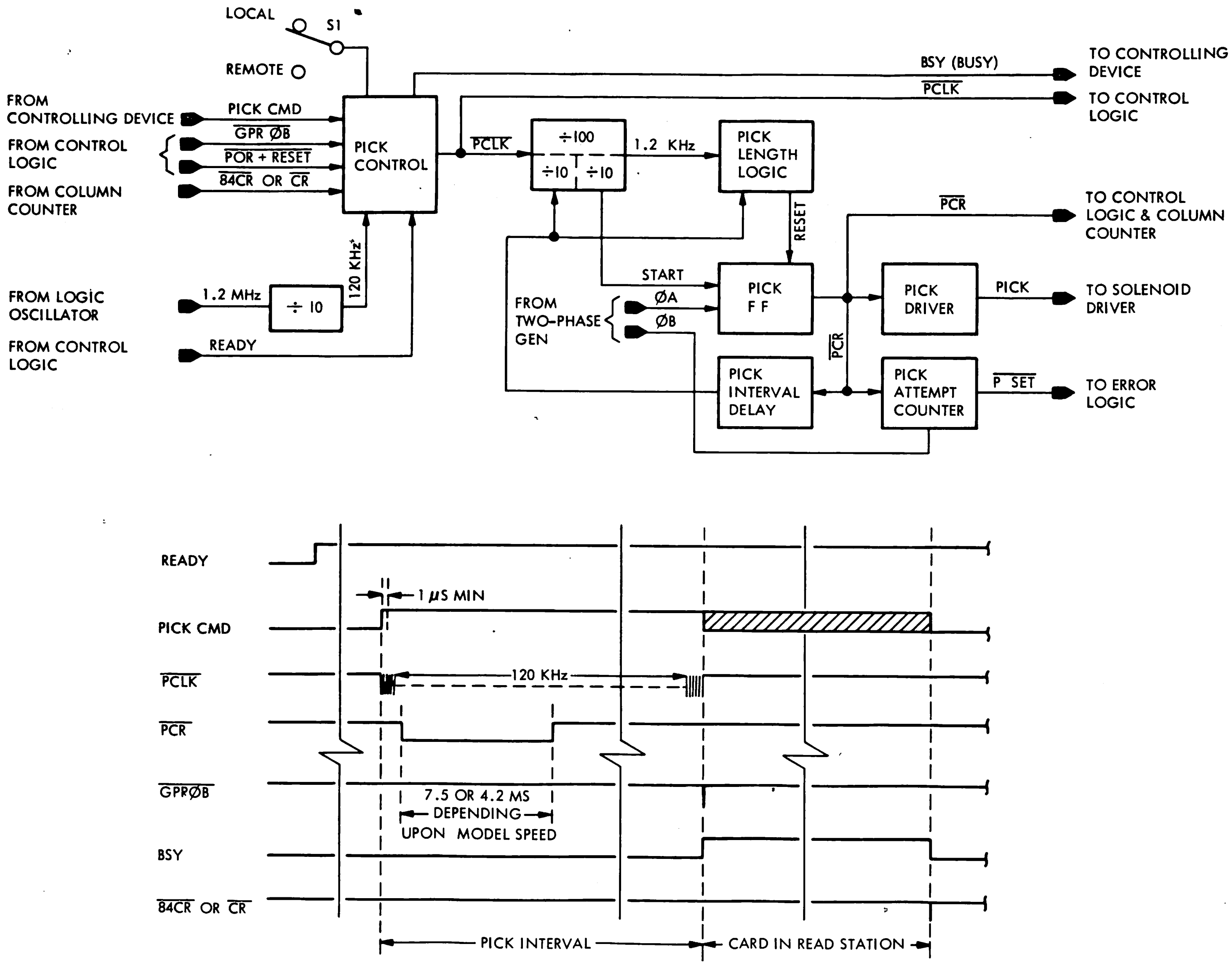


Figure 14. Pick Logic Diagram and Timing

5. If the leading edge has not arrived in 50 ms, generate another pick pulse.
6. Repeat the pick attempt six times and if the leading edge has not appeared, generate a pick fail alarm ($\overline{\text{PSET}}$).

The Pick Control generates $\overline{\text{PCLK}}$ (Figure 14 timing) until a $\overline{\text{GPR ØB}}$ is received or READY goes false due to the pick fail signal or $\overline{\text{P SET}}$. $\overline{\text{PCLK}}$ gated from Pick Control is divided by two decade MSI counters to a frequency of 1.2 KHz. The first decade counter provides a Start (set) signal to the Pick Flip Flop on its second count. This begins the PICK pulse internal. The 1.2 KHz from the second decade counter then drives the four-stage binary pick length logic counter until a preselected count is decoded. When decoded, the count resets the Pick Flip-Flop and ends the PICK pulse.

At the end of the PICK pulse, signal $\overline{\text{PCR}}$ initiates the Pick Interval Delay of 50 ms. During this delay period, the ÷ 100 and Pick Length Logic is held reset while the Pick Control waits for a $\overline{\text{GPR ØB}}$. A $\overline{\text{GPR ØB}}$ signals the the entry of a card into the read station and therefore no more pick attempts should be made. If $\overline{\text{GPR ØB}}$ has not been received by the end of the delay, another PICK pulse is generated. This process is repeated until $\overline{\text{GPR ØB}}$ occurs or the Pick attempt counter reaches count six and a $\overline{\text{P SET}}$ is generated. $\overline{\text{P SET}}$ will cause READY to go false terminating $\overline{\text{PCLK}}$.

Upon receipt of a $\overline{\text{GPR ØB}}$, the Pick Control signals BSY (Busy) to the controlling device to indicate a card has entered the read station. BSY remains true until $\overline{\text{84 CR}}$ or $\overline{\text{CR}}$ indicating the card has left the read station and another PICK CMD will be accepted.

The positioning of switch S1 determines the source for the PICK CMD. In local, the PICK CMD signal is held true so that whenever the reader is READY, PICK CMDs are generated internally each time 84 CR or CR is reached. When in REMOTE, only a PICK CMD from the controlling device can initiate a read cycle.

Column Counter

The Column Counter (Figure 15) tracks the card's movement as it passes through the read station by counting magnetic pulses generated by a timing disk mounted to the first capstan roller's shaft. This capstan roller engages the card as it is released by the picker and thereafter determines the speed at which the card will move through the read station. The timing disk provides two pulses for each .087 inch column and therefore provides .043 inch resolution. To improve this resolution to .022 inch, the 180° Phase Shift Logic is used. When a card enters the read station, $\overline{\text{GPR ØB}}$ is generated and used to

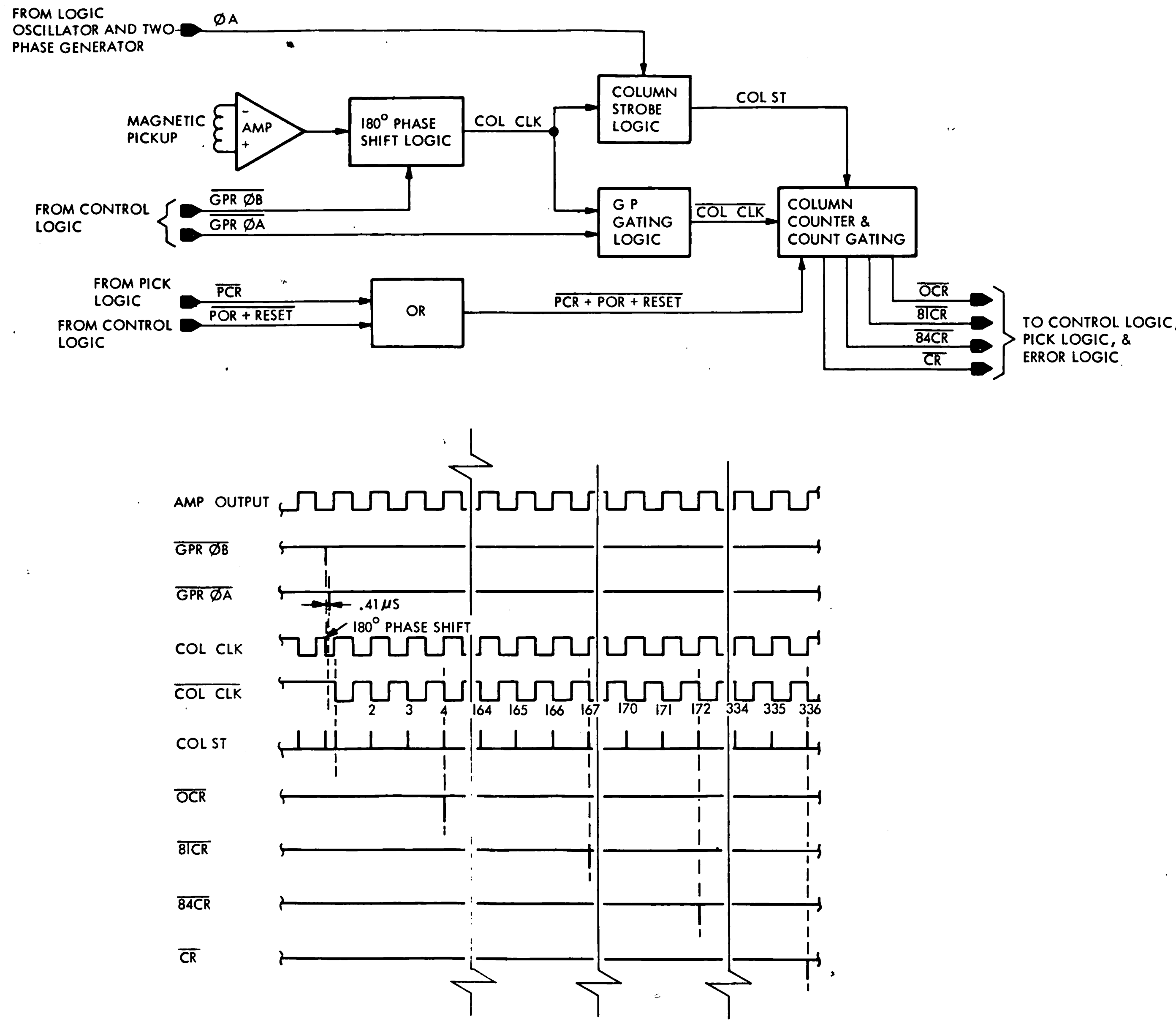


Figure 15. Column Counter Diagram and Timing

sample the AMP's output signal. If the AMP's output is low, a 180° shift will occur. If the AMP's output is high, no phase shift occurs. In effect, this logic causes the AMP's output signal to always be high when a card is detected in the read station.

$\overline{\text{GPR ØB}}$ is followed in .41 us by $\overline{\text{GPR ØA}}$. Receipt of $\overline{\text{GPR ØA}}$ by the GP Gating Logic gates $\overline{\text{COL CLK}}$ to the Column Counter and count Gating. The Column Strobe Logic provides a delayed strobe pulse each time COL CLK goes positive. This strobe checks the Count Gating to determine if the counter has reached $\overline{\text{OCR}}$, $\overline{\text{81 CR}}$, $\overline{\text{84 CR}}$ or $\overline{\text{CR}}$. These signals are used by the Control Logic, Pick Logic and Error Logic as follows:

<u>COUNT</u>	<u>USED BY</u>
$\overline{\text{OCR}}$	1) Data Control to set the IMFF Flip Flop 2) Error Logic for an All Zeros Check
$\overline{\text{81 CR}}$	1) Data Control to Reset the IMFF Flip Flop 2) Error Logic for an All Zeros Check 3) Error Logic for an Stack Check
$\overline{\text{84 CR}}$	1) Control Logic to reset the RESET INHIBIT Flip Flop 2) Pick Logic to enable the Pick Control for the next PICK CMD. 3) Error Logic for an All Zeros Check
$\overline{\text{CR}}$ (M 300 only)	1) Control Logic to reset the RESET INHIBIT Flip Flop 2) Pick Logic to enable the Pick Control for the next PICK CMD.

The Column Counter continues its count until $\overline{\text{PCR}}$ is received from the Pick Logic or until count 384 is reached. At count 384 all further $\overline{\text{COL CLK}}$ is inhibited from driving the Column Counter and Count Gating.

Data Control

The Data Control logic (Figure 16) is reset each time a card enters the read station and a $\overline{\text{GPR ØB}}$ is generated. $\overline{\text{OCR}}$ from the Column Counter then sets the IM Flip Flop which releases the CLOCK input to the Clock Filter and MSMV via a wired OR. (The Clock line is held to ground during all intervals of

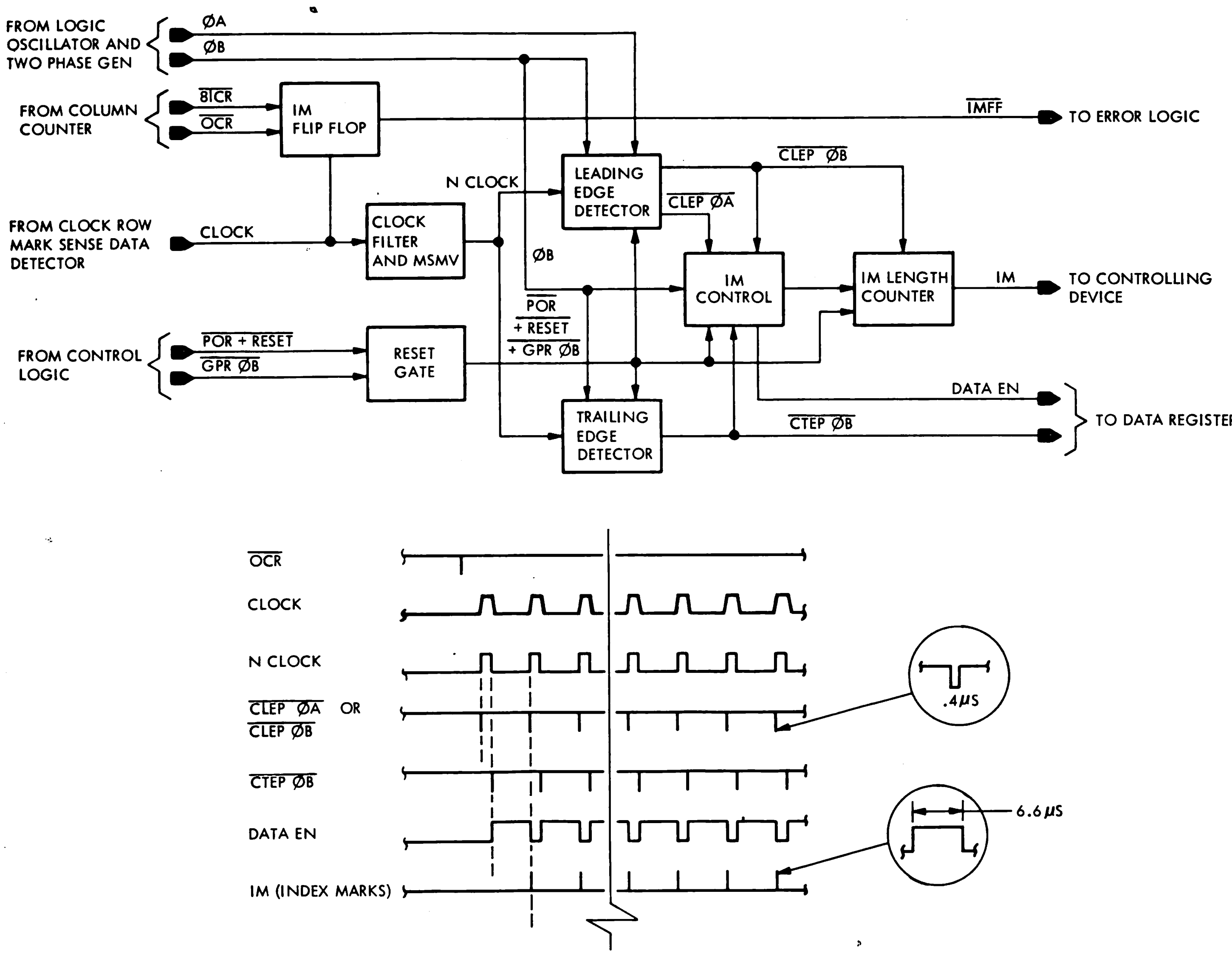


Figure 16. Data Control Diagram and Timing

non-reading to prevent erroneous IM pulses. This is of necessity due to the design of the Mark Sense Data Detectors and the fact that no surface reflectance reference is available when no card is in the read station.)

CLOCK signals generated by the Clock Row Mark Sense Data Detector are filtered by the Clock Filter and used to trigger the Schmitt-Trigger input of the MSMV. The MSMV then generates N CLOCK which drives the leading and trailing edge Detectors. These then generate signals CLEP ØA, CLEP ØB and CTEP ØB as shown in the timing of Figure 16. CLEP ØB is used to reset the IM Control and Length Counter just prior to CLEP ØA. The first CLEP ØA (N Clock Leading Edge Pulse ØA) is used to precondition the IM Control so that the second CLEP ØA will generate an IM Index Mark and reset DATA EN. The trailing edge of the first N CLOCK generates CTEP ØB (N Clock Trailing Edge Pulse ØB). CTEP ØB sets a Flip Flop in the IM Control enabling the DATA EN signal and also resets the Data Register. While DATA ENABLE is high all marks or punches detected by the Mark Sense Data Detectors will be transferred to the Data Register. The second N CLOCK generates CLEP ØA number two which resets DATA EN and initiates an IM. The IM Control delays the start of the IM for 1.2 us after DATA EN goes false in order to guarantee data settling on the output lines before the controlling device receives the IM. The IM length Counter counts gated ØB pulses until Count 4 is decoded providing a 6.6 us IM to the controlling device. The trailing edge of the second N CLOCK will again set the DATA EN signal and mark the end of the guaranteed data interval (from CLEP ØA to CTEP ØB).

This process is repeated for each clock mark detected until 81 CR occurs. 81 CR resets the IM Flip Flop and holds the CLOCK line to ground.

Error Logic

The Error Logic of Figure 17 contains the error/alarm detection circuits and the Ready Gate.

Once a PICK CMD is accepted by the reader, the Error Logic is sampled at intervals of card processing for error and reader conditions. The first test is Pick Check. If a P SET is signalled to Pick Check, a MOCK Motion Check will be sent to the controlling device. P SET will occur approximately 300 ms after PICK CMD was received and reader READY will be reset. Pick Check will be signalled to the operator by the PICK CHECK control panel indicator. If PICK CHECK does not occur, a ready cycle will be in process and OCR will sample the All Zeros Check circuits. Should ONE "1" be present during the check, indicating a failed Mark Sense Data Detector or a torn card leading edge, an

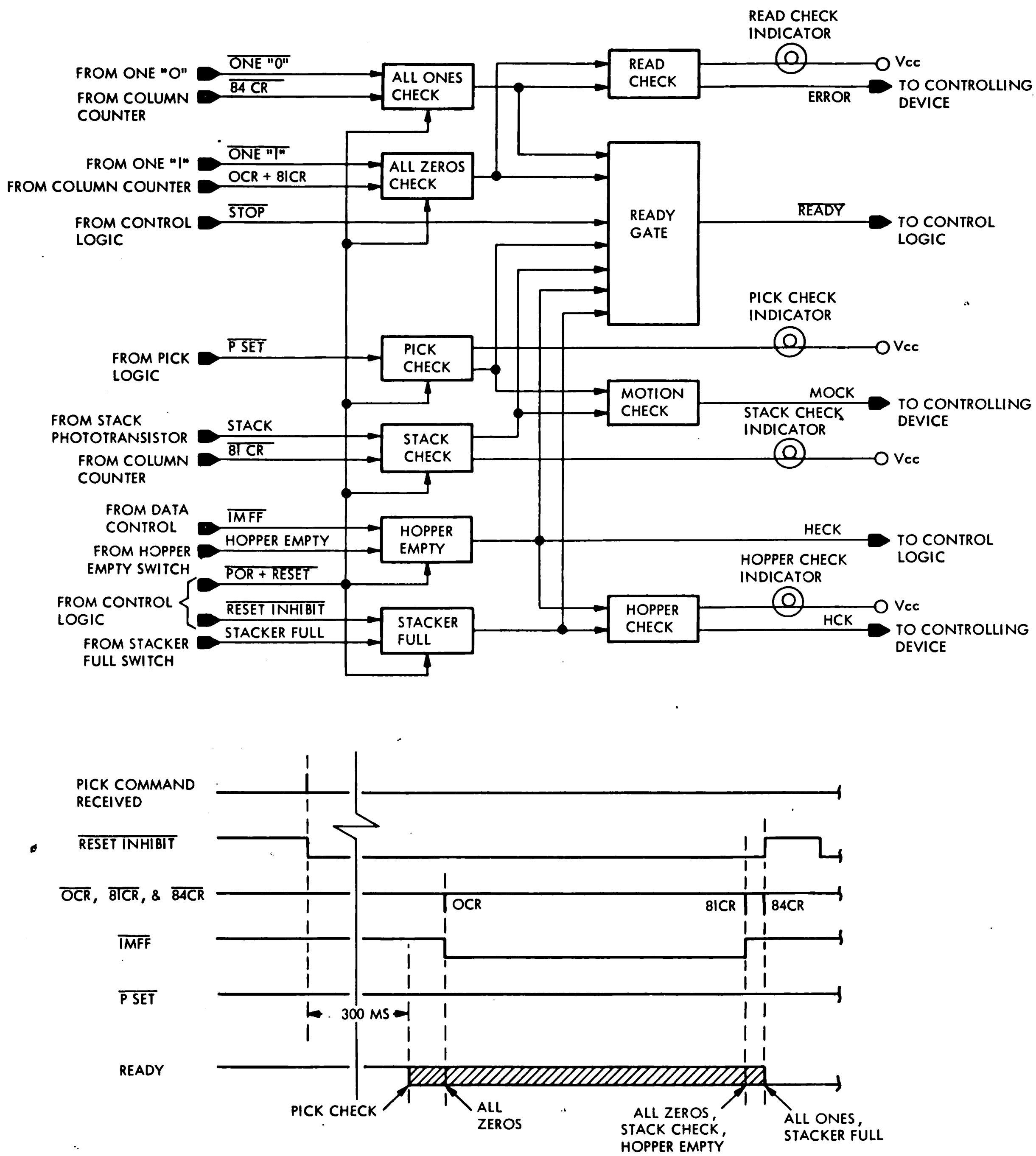


Figure 17. Error Logic Diagram and Timing

ERROR signal will be sent to the controlling device and the READY dropped. The reader control panel will indicate Read Check.

OCR will be followed by $\overline{\text{81 CR}}$ which again samples the All Zeros Check circuits and the Stack Check circuits. The stack check sensor is located at the exit of the card track and detects that the tail of a card is clear of the card track (hence, fully seated in the output stacker). The Stack Check Logic is designed to test the stack sensor dark-to-light transition (i.e., track clear) between the time an 81 CR signal occurs (card tail leaving the read station) and the OCR signal of the next card. Should this transition not have taken place, a STACK CHECK alarm is generated. This signal generates a MOTION CHECK to the controlling device, resets the READY line and lights the Stack Check indicator on the control panel.

Since $\overline{\text{IMFF}}$ is reset by $\overline{\text{81 CR}}$, the Hopper Empty circuit will be checked for closure of the hopper empty microswitch. This switch is located in the riffle cap and senses when the last card has left the Hopper. If the hopper is empty at $\overline{\text{81 CR}}$, HCK (Hopper Check) is signalled to the controlling device and READY is reset. Hopper Check is signalled to the operator by the Hopper Check Indicator.

$\overline{\text{84 CR}}$ occurs next in the read cycle and samples the All Ones Check circuitry. A $\overline{\text{ONE "O"}}$ present at $\overline{\text{84 CR}}$ indicates a failed Mark Sense Data Detector or excessive card slip in the read track. This error is signalled to the controlling device as an ERROR and the READY line is reset. Visual indication is generated by the Read Check Indicator.

Since $\overline{\text{84 CR}}$ is also used to reset $\overline{\text{RESET INHIBIT}}$, the Stacker Full circuit will be checked for a closure of the Stacker Full Switch. If the switch is closed, the Stacker Full circuitry will send HCK to the controlling device. reset READY, and light the Hopper Check Indicator.

All error conditions are cleared by the Reset Switch.

<u>DATA DETECTION</u>

The following is a detailed description of each block shown under Data Detection in Figure 11 Block Diagram - OM Series Card Reader.

Mark Sense Data Detectors

Light from the Light Station is reflected from the card's surface and optically coupled to the Read Station's phototransistors by glass fibers. Glass fibers of .002 inches in diameter are packed together to form a window of .010

inches by .100 inches for each of the 13 Mark Sense Data Detectors. These windows scan the card's surface from .007 inches to .010 inches away coupling the reflected light to the phototransistors. All phototransistor collectors are bussed together and connected to +5 VDC. Each phototransistor's emitter is connected to its Mark Sense Data Detector. Figure 18 is a Block Diagram and shows a typical waveform for reflected signals and recovered data for the Mark Sense Data Detectors.

Light reflected into the fiber optics window for Row 12 is coupled to the base of Row 12's phototransistor. The phototransistor's emitter is coupled through R2 to an operational amplifier Voltage Follower. The Voltage Follower combined with D1 and Ref. Storage track and store the positive peaks from the phototransistors emitter. This stored voltage is subsequently divided by a resistor network and used to established the reference for the Voltage Comparator. The reference is dumped (reset) to ground by the Ref. Dump FET each time a DRD pulse is received. DRD pulses are generated on the leading edge of each clock mark and therefore a new reference voltage is established between each data column.

The waveform of Row 12 in Figure 18 shows the reference voltage superimposed on the Phototransistor's emitter output. Whenever the input voltage through R3 to the Voltage Comparator operational amplifier drops below the reference voltage due to a pencil mark or a punched hole, the Voltage Comparators output will go high producing a true data condition (data one). The D Row 12 waveform shows the detected data.

Rows 11 through 9 function identically to ROW 12. The CLOCK ROW data is detected in an identical manner, however the Clock's Ref. Dump circuit receives its dump signal (CRD) on the trailing edge of each clock mark.

Good Pick Detector

To initiate the synchronization process between the card movement and the reader electronics, a GP ENABLE is generated by the Good Pick Detector. The GP ENABLE signal is used by the Control Logic to generate a $\overline{\text{GPR }\emptyset\text{B}}$ and $\overline{\text{GPR }\emptyset\text{A}}$. These signals reset the Pick Logic and enable the Column Counter.

The Good Pick Detector (Figure 19) receives inputs from the phototransistor emitters for ROWS 12, 0, 4, 7 and 9. These inputs form a diode OR at the input of the Good Pick Detectors voltage comparator. As the card enters the read station, the first phototransistor to receive reflected light from the card surface will generate the waveform shown for ROW 12, 0, 4, 7 or 9.

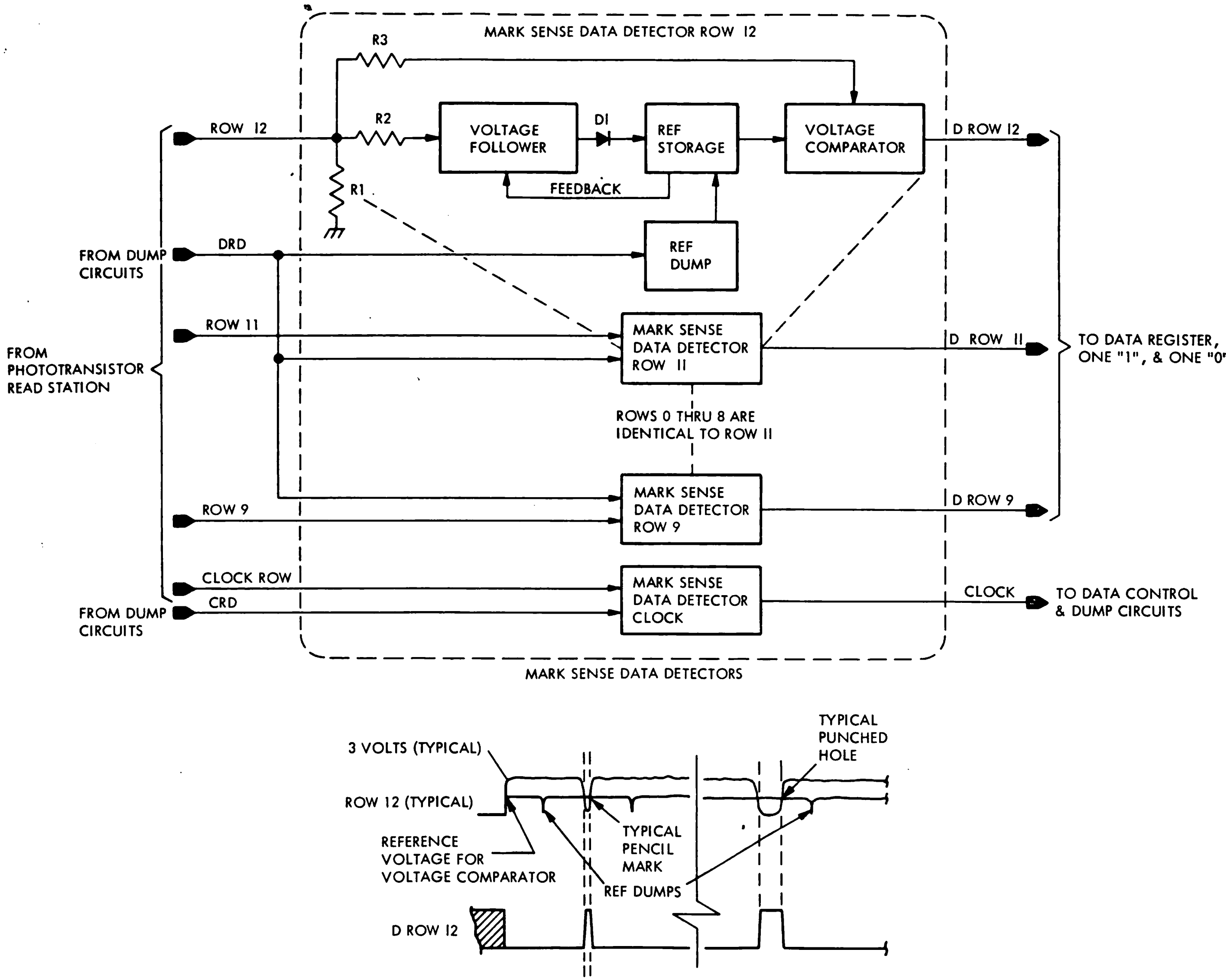


Figure 18. Mark Sense Data Detectors

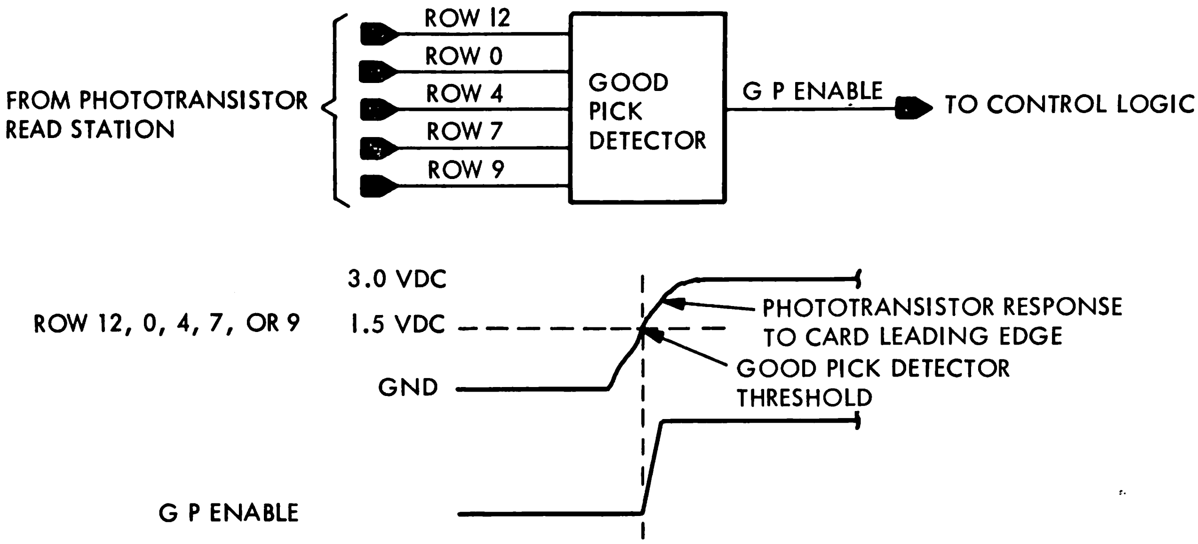


Figure 19. Good Pick Detector and Timing

When the voltage crosses the threshold of approximately 1.5 volts, the voltage comparator will generate the GP ENABLE waveform.

Dump Circuits

As the card passes the Read Station, the clock marks are detected, amplified by logic inverters and used to drive the Dump Circuits.

Figure 20, Dump Circuits and Timing shows the timing relationship of CLOCK to DRD (Data Reference Dump) and CRD (Clock Reference Dump). The Mark Sense Data Detector for the clock row receives the waveform CLOCK ROW and generates CLOCK. CLOCK is buffered by Logic Buffers and then drives the Data Reference Dump and Clock Reference Dump circuits. Both Reference Dump circuits are AC coupled, PNP transistor amplifiers that turn ON when the negative edge of CLOCK or $\overline{\text{CLOCK}}$ are received. The resulting signals DRD and CRD are as shown in Figure 20.

One "1" and One "0"

In order to provide the All Zeros Check at OCR and 81 CR and the All Ones Check at 84 CR, the outputs of the 12 Mark Sense Data Detectors (D ROW 12 THRU D ROW 9) are OR'ed in the ONE "0" nand gate and AND'ed in the ONE "1" nor gate.

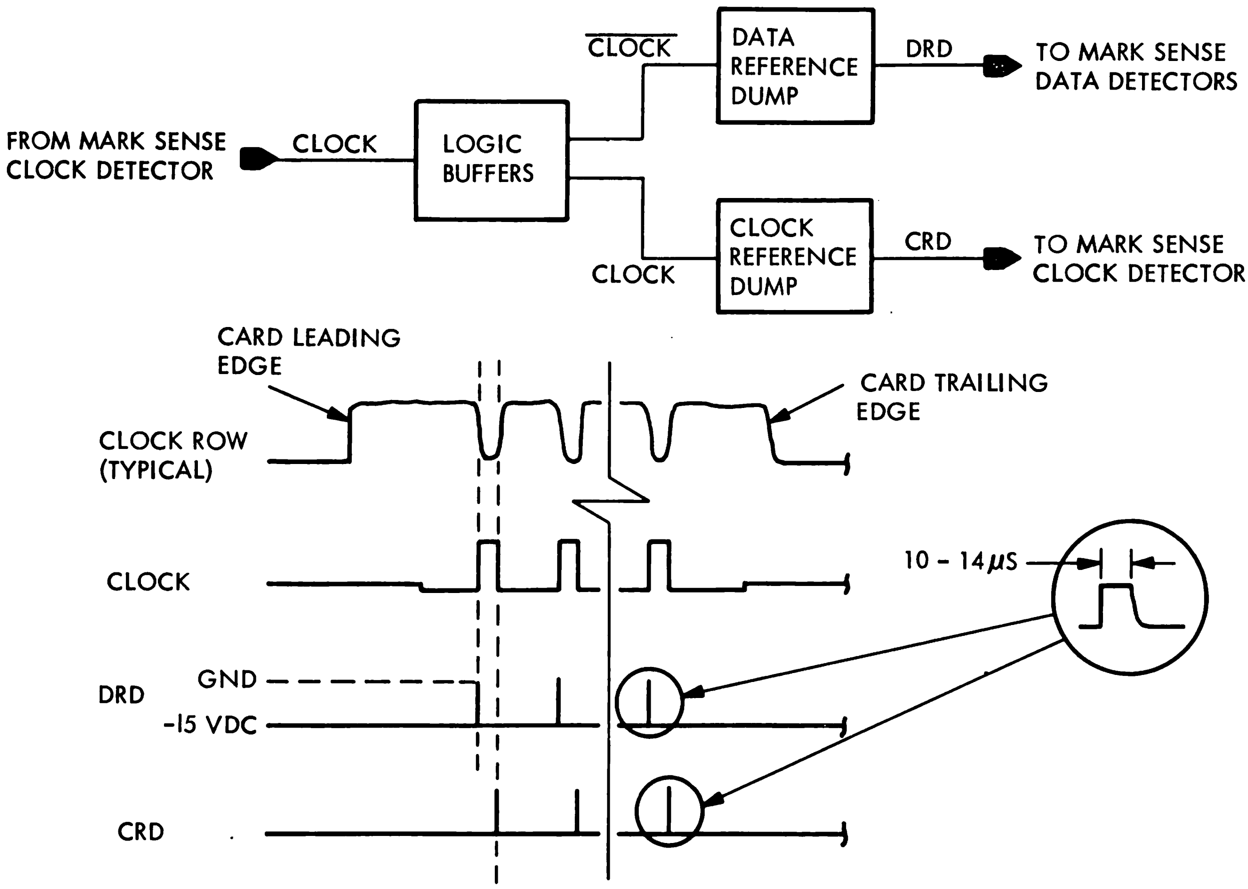


Figure 20. Dump Circuits Diagram and Timing

The timing of Figure 21 shows the normal waveforms for $\overline{\text{ONE "1"}}$ and $\overline{\text{ONE "0"}}$. When OCR occurs, $\overline{\text{ONE "1"}}$ should be high indicating no data was being detected. The same is true at 81 CR. AT 84 CR $\overline{\text{ONE "0"}}$ should be high indicating all ones are being detected by the Mark Sense Data Detectors. If either $\overline{\text{ONE "1"}}$ or $\overline{\text{ONE "0"}}$ is true (LOW) at OCR, 81 CR or 84 CR, a Read Check will result and reader READY will be reset.

Data Storage

The following describes the blocks shown under Data Storage in Figure 11 Block Diagram - OM Series Card Reader.

Data Register and Data Drivers

Data detected by the Mark Sense Data Detectors is stored in the Data Register for transfer through the Data Drivers to the Controlling Device. Figure 22, Data Register and Data Drivers Diagram and Timing details this sequence.

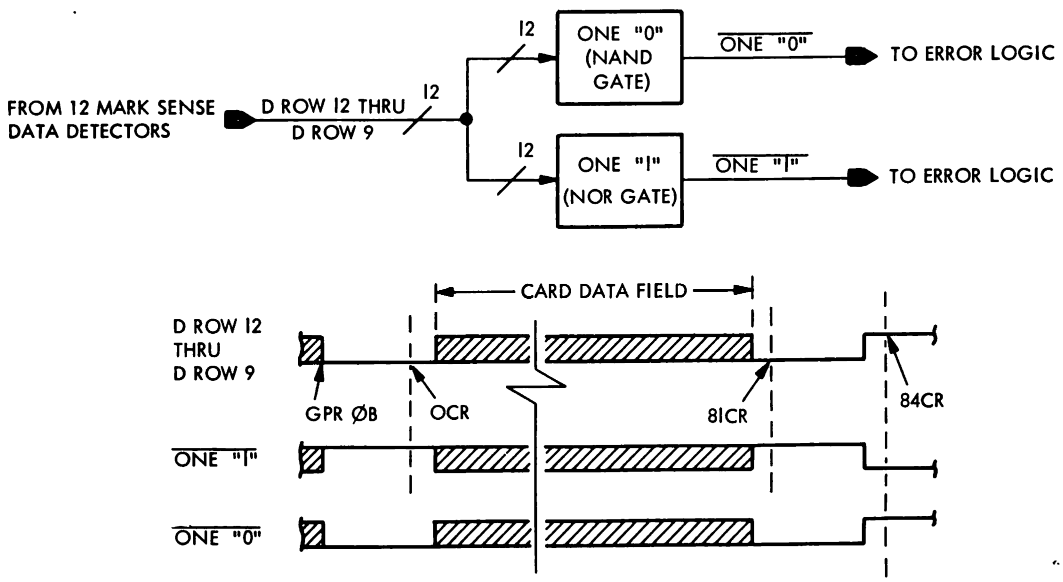


Figure 21. One "1" and One "0" Diagram and Timing

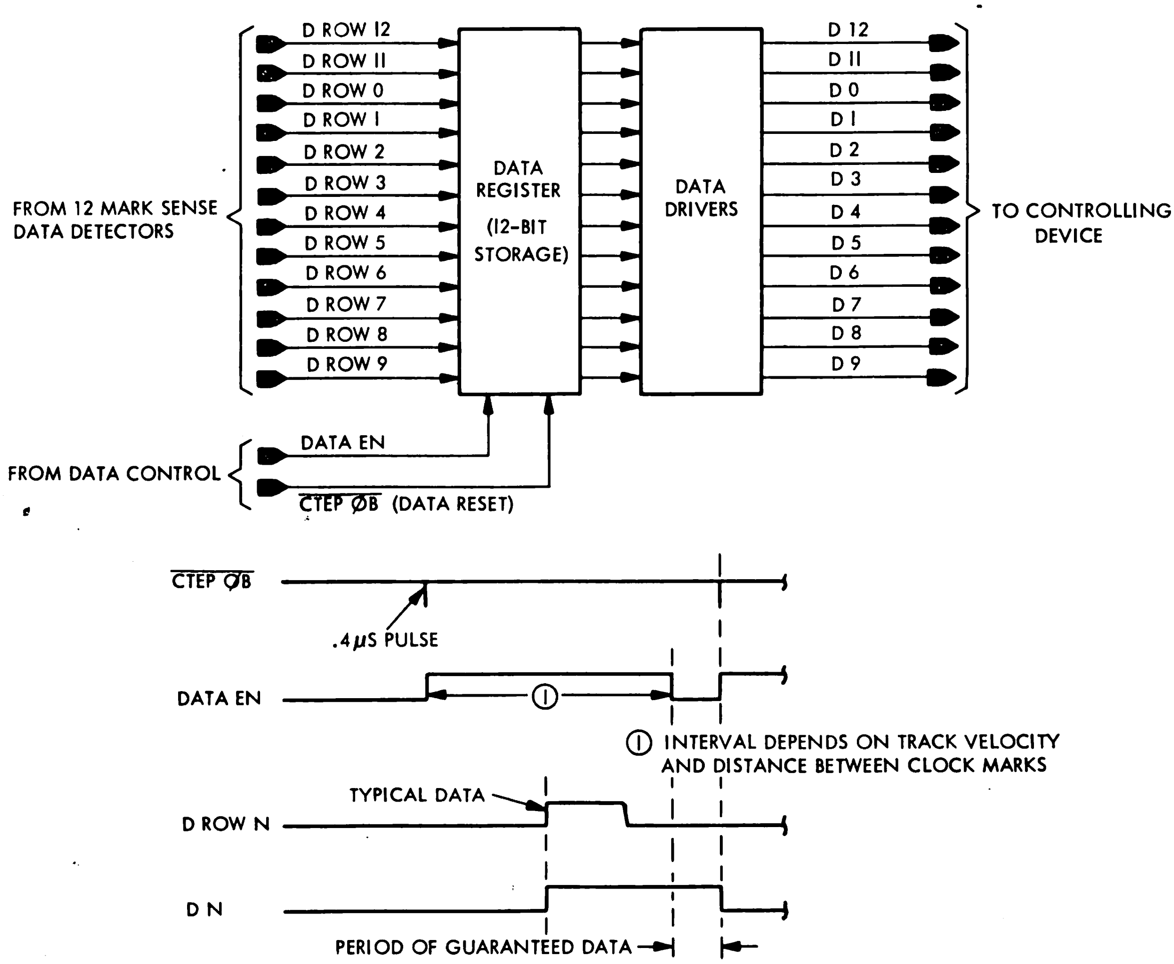


Figure 22. Data Register and Data Drivers Diagram and Timing

The 12 bit Data Register is reset each time $\overline{\text{CTEP }\emptyset\text{B}}$ is generated by a clock mark. Coincident with $\overline{\text{CTEP }\emptyset\text{B}}$ the DATA EN signal becomes true allowing storage of detected data (see example shown in Figure 22's timing). Any D ROW input that is high during DATA EN will cause a "1" to be stored for its row. The end of the DATA EN period is generated by detection of a clock mark's leading edge. While DATA EN is low, no more data can enter the register thus giving a period of guaranteed data from DATA EN going low until another $\overline{\text{CTEP }\emptyset\text{B}}$ is generated resetting the data.

The Data Drivers provide the necessary buffering between the Data Register and the Controlling Device.

REPLACEMENT OF STACKER PHOTOCELL

1. Perform steps 1 and 2 of Replacement of Hopper Empty Switch.

2. Using a 1/16 Allen screwdriver, LOOSEN set screw in stacker casting holding stacker photocell, Figure 43.

3. Remove photocell from casting, Figure 43, and tag black and white wires from photocell.

4. Replace photocell, align photocell flush with stacker casting face-plate, and tighten photocell set screw, Figure 43. Replace leads.

5. Reassemble reader in reverse order of disassembly.

REPLACEMENT OF READ STATION

1. It is necessary to remove the main mounting plate for this repair. Perform steps 1 through 13 of Replacement of Belt on Vacuum Pump Motor Assembly.

2. Remove tie-wraps on solenoid mounting plate.

3. Remove four phillips head 4-40 screws (1), Figure 47, holding Read & Light Station Assembly in pick casting.

4. Using a 1/16" Allen wrench turn out the four adjustment set screws (2) 1/4 inch, Figure 47.

5. Slide Read and Light Station up and out of the pick casting.

6. Remove tie-wraps from cable assembly.

7. Remove four 4-40 flat head Phillips screws (1) holding the Read Station to the Light Station, Figure 48.

8. Unsolder Read Station wires from Read Station.

9. Replace Read Station and resolder wires to the new Read Station.

10. Reassemble in reverse order of disassembly leaving reader top cover off.

11. By adjusting socket head screws (2) and Phillips head screws (1), Figure 47, position the Read and Light Station assembly so two card thicknesses fit snugly between the Read and Light Station and the Stack Casting wall, Figure 47. To make sure both top and bottom are properly adjusted, adjust bottom first.

NOTE

Following Replacement of the Read Station, the Read Station's phototransistors must be checked for proper Light voltages with an oscilloscope or high impedance (1 meg ohm or greater) voltmeter.

12. Place Data Card, P/N 1540872, on extender board.

13. Remove power from the Reader's drive motor by disconnecting the motor's AC connector (Figure 38).

14. Turn the reader on and hand feed a mark sense card (blank surface forward) about half way through the Read Station. (Make sure card lying straight in the card track.)

15. Measure light voltages for all rows and record.

Row	Data Card I/O Pin	Data Card Resistor
12	H	R11
11	K	R28
0	5	R42
1	7	R63
2	M	R77
3	9	R91
4	3	R18
5	P	R35
6	16	R49
7	E	R70
8	15	R84
9	1	R98
CLOCK	C	R56

16. All rows should produce voltages from 1.3V to 4.0V with a maximum spread of 2 volts, i.e., if the lowest channel is 1.3 volts, the highest should be less than or equal to 3.3 volts.

17. If one or more rows are out of the voltage range, select-at-test (SAT) resistors should be used to replace the nominal 10K ohm resistors (see table under step 15). SAT resistor range is 4.7K ohm to 15K ohm. Increasing the resistors' value will increase the light voltage. Decreasing the resistors' value will decrease the light reading.

18. Place cover on Reader.

REPLACEMENT OF LIGHT STATION BULB

1. It is necessary to remove the main mounting plate for this repair. Perform steps 1 through 13 of Replacement of Belt on Vacuum Pump Motor Assembly.

2. Remove fastons from bulb, unscrew bulb and replace. Be sure rubber washer remains inside bulb housing, Figure 48.

3. Place fastons on new bulb and reassemble reader.

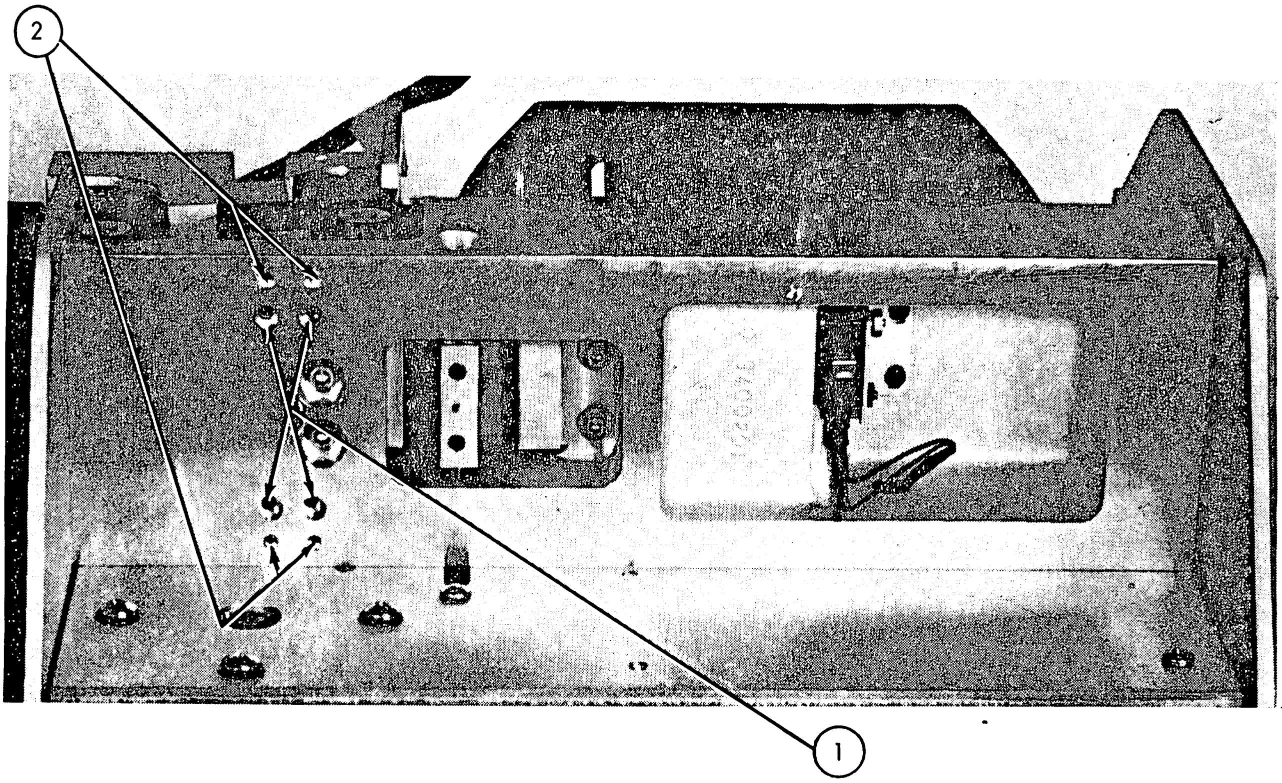


Figure 47. Read and Light Station Mounting and Adjustment Screws

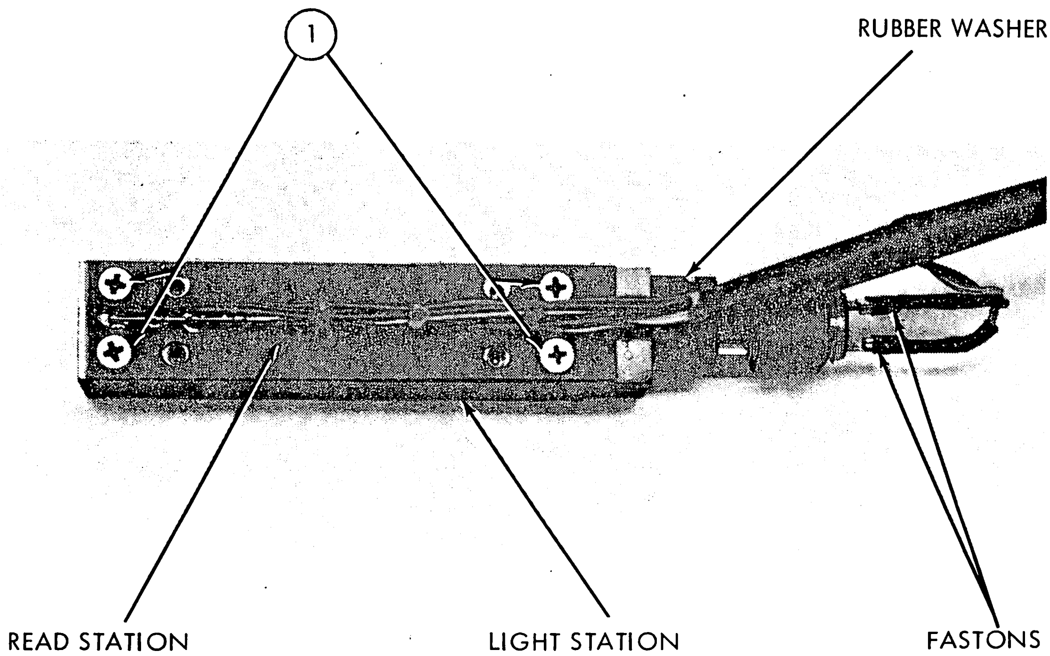
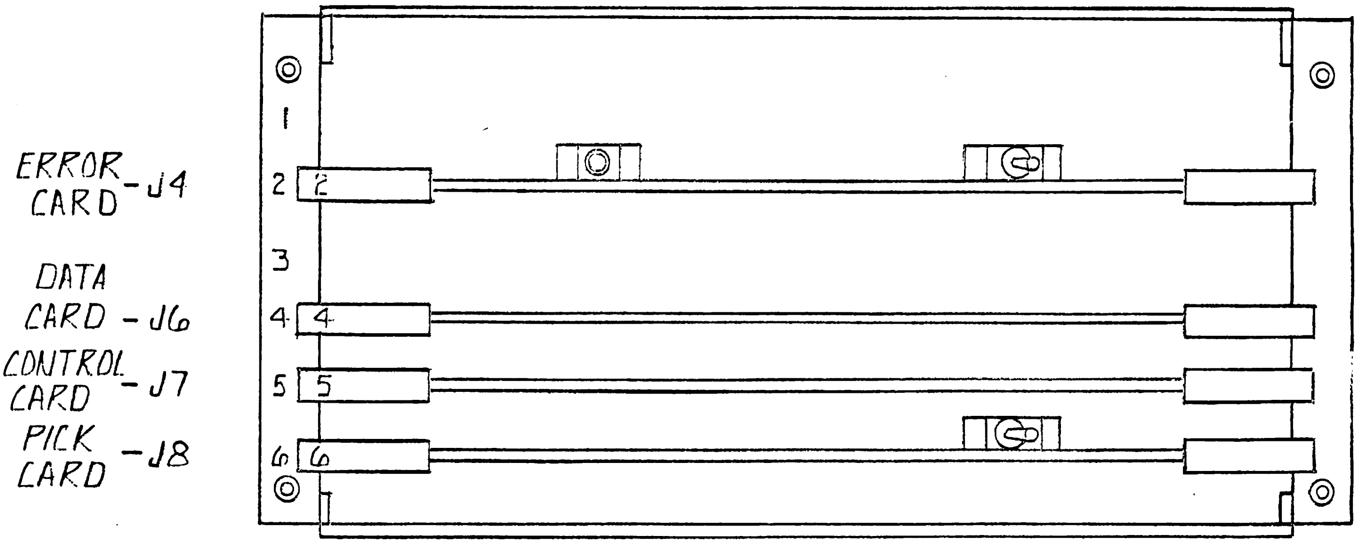
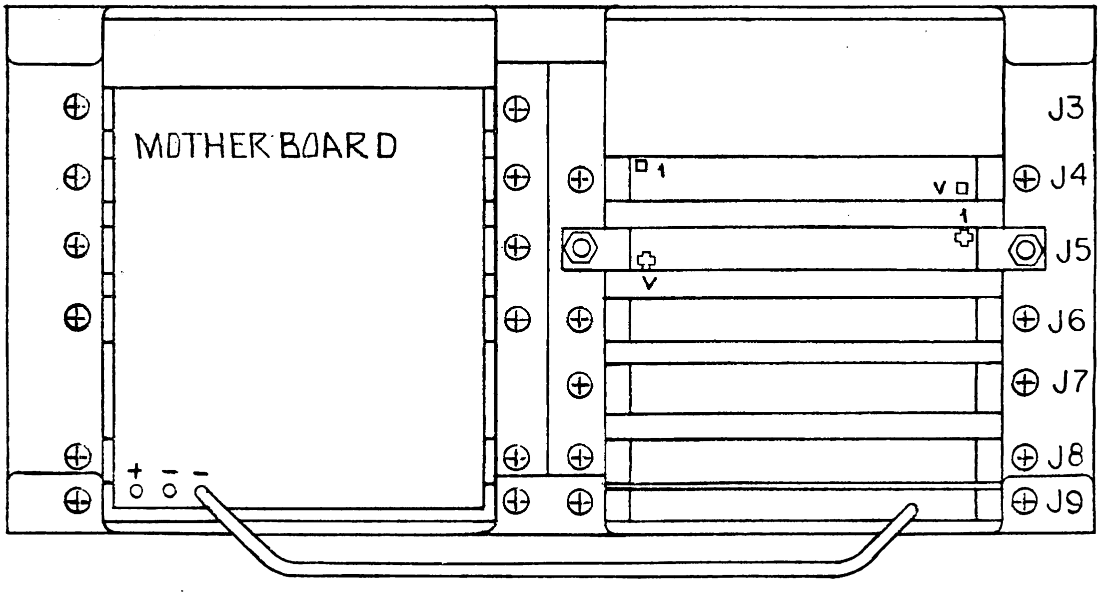


Figure 48. Read and Light Station Assembly



CARD FILE, REAR VIEW
COVER REMOVED



CONNECTOR VIEW

Figure A4. Card File

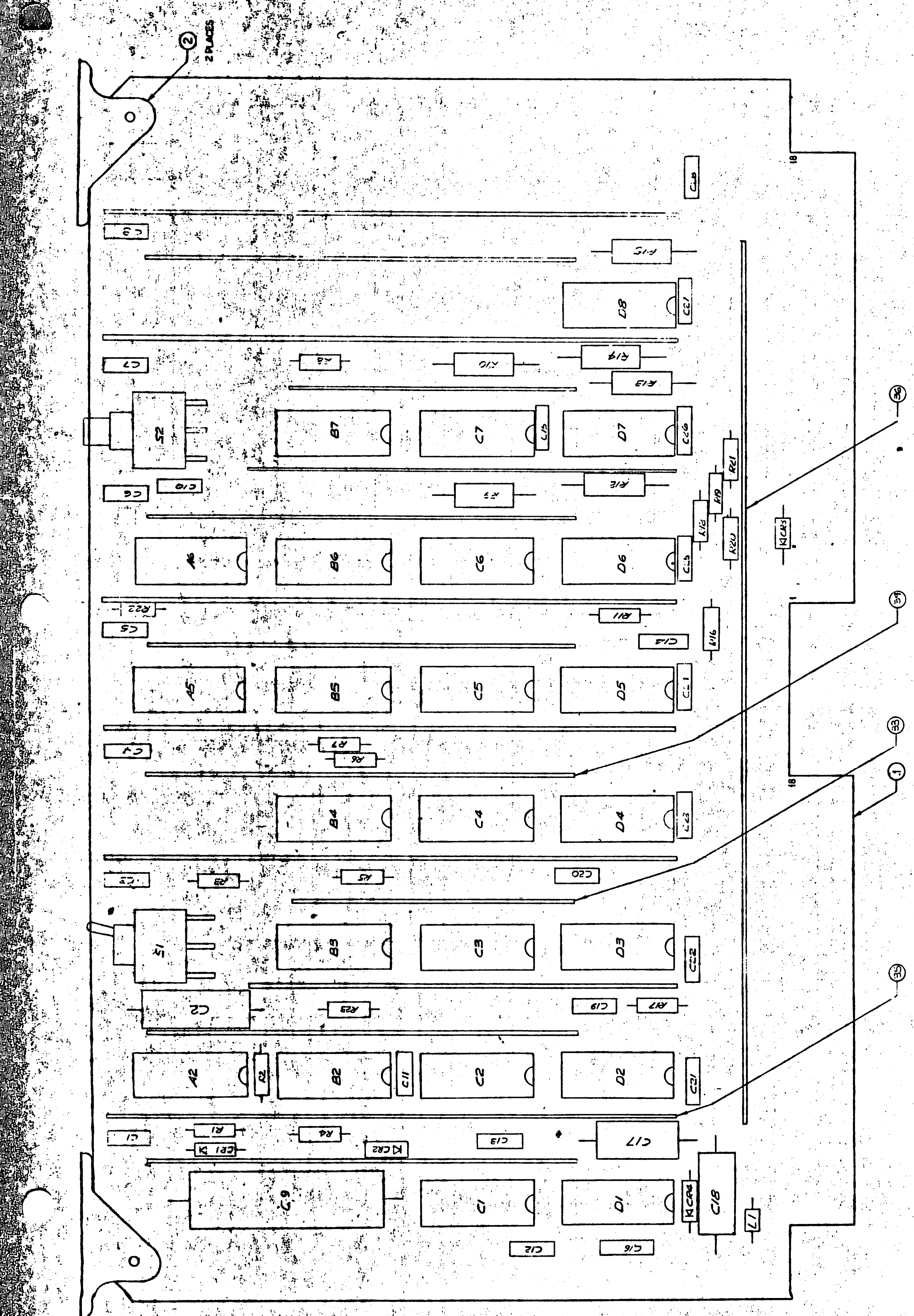


Figure A5. Error Card Assembly - Dwg. No. 1540899

MB- MB- MB- MB- MB- MB- MB

D5
D6
B6
B7
C7
B8

B5
D8
B9
D4
C9
B4

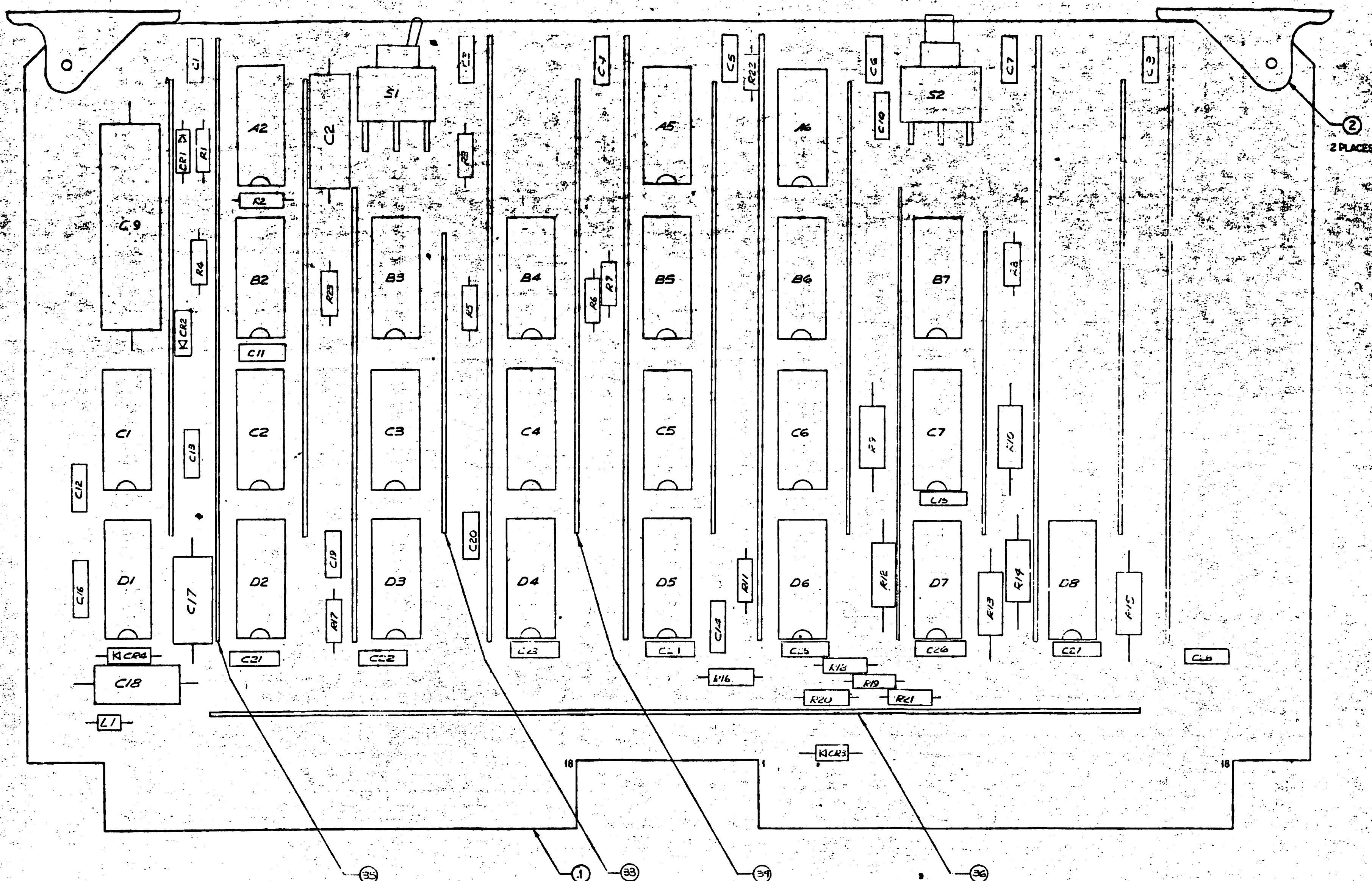


Figure A5. Error Card Assembly - Dwg. No. 1540899

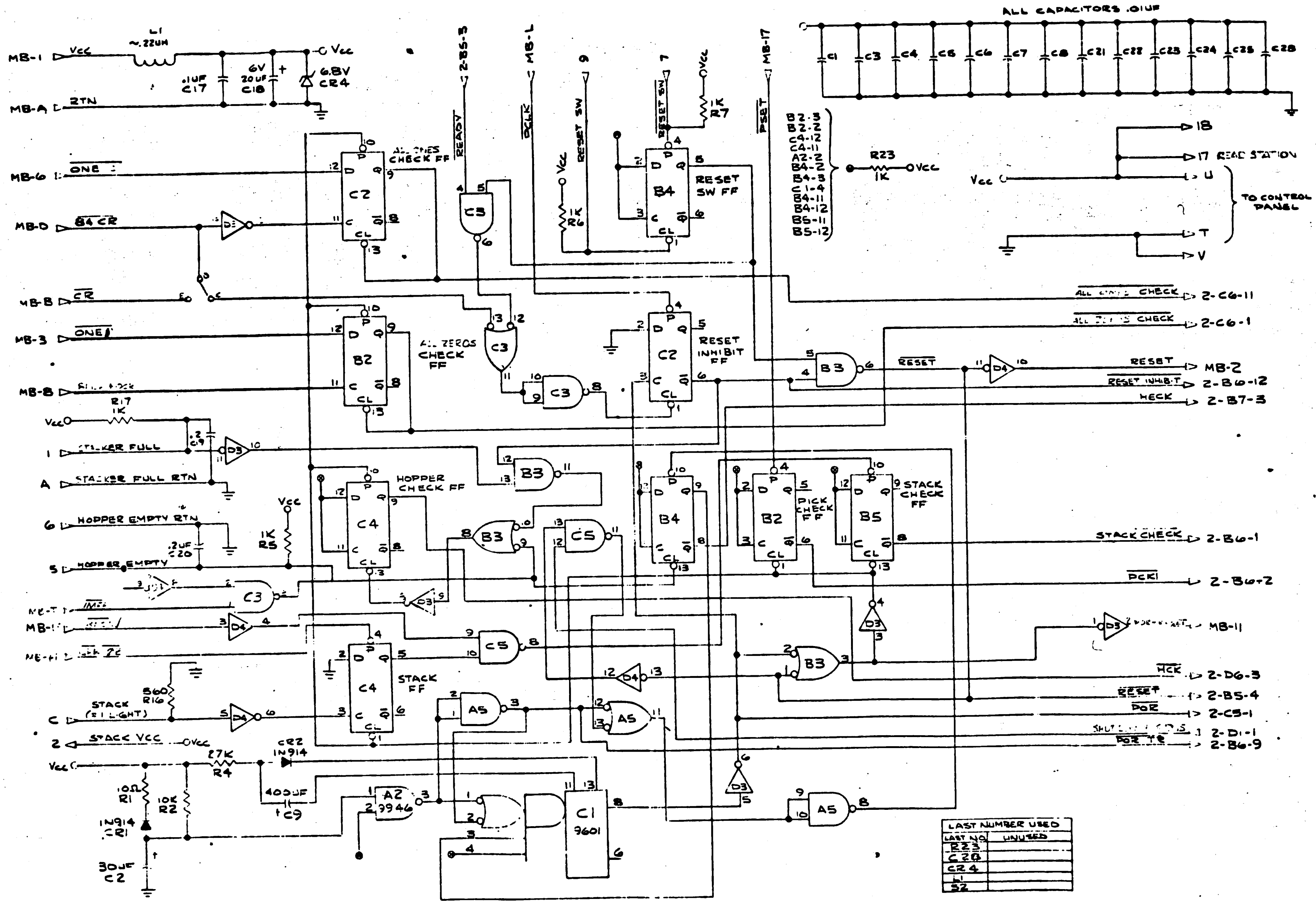


Figure A6. Error Card Schematic (sheet 1 of 2)
(Dwg. No. 1541375)

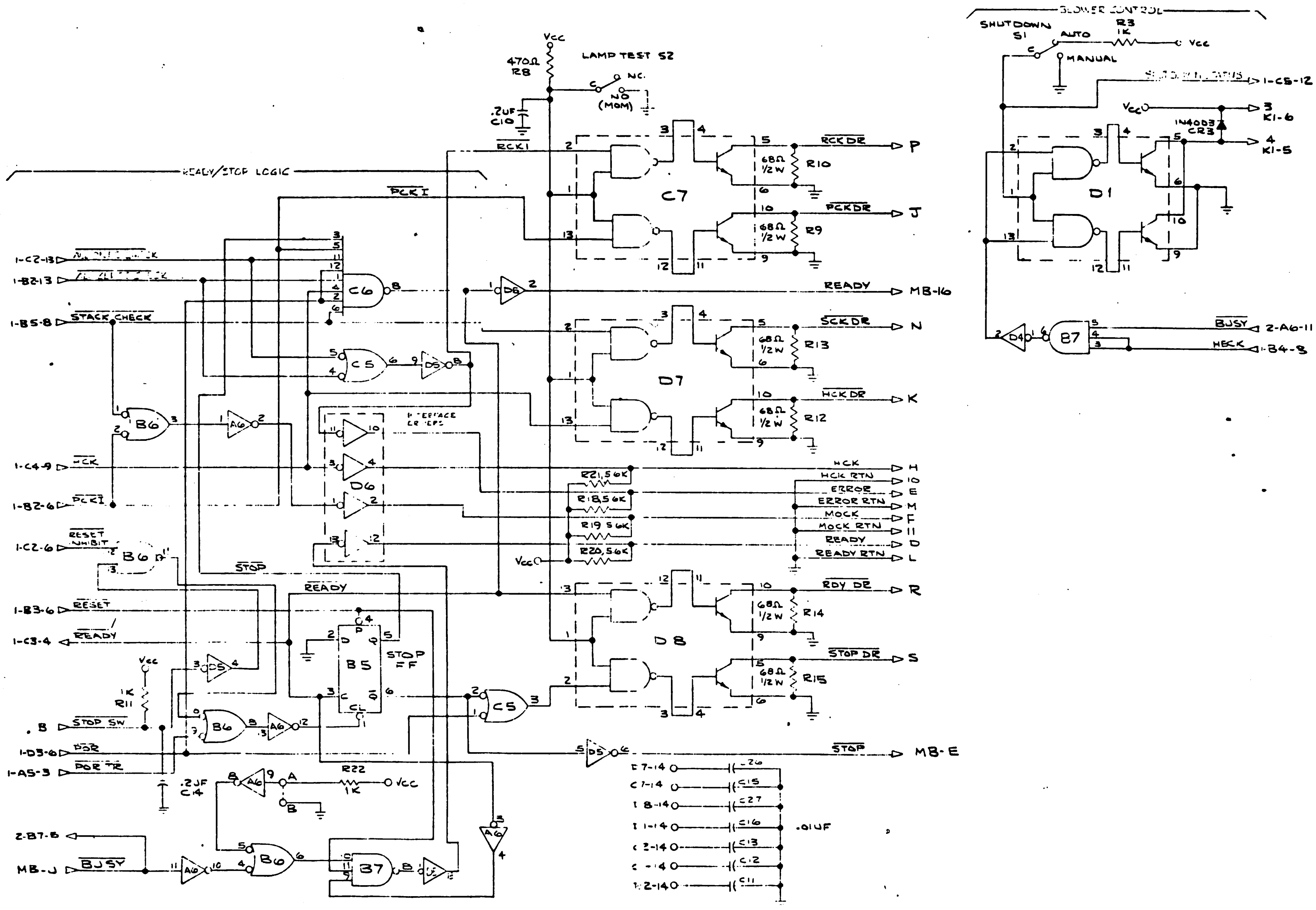


Figure A6. Error Card Schematic (sheet 2 of 2)

D5
D6
B6
B7
C7
B8

B5
D8
B9
D4
C9
B4

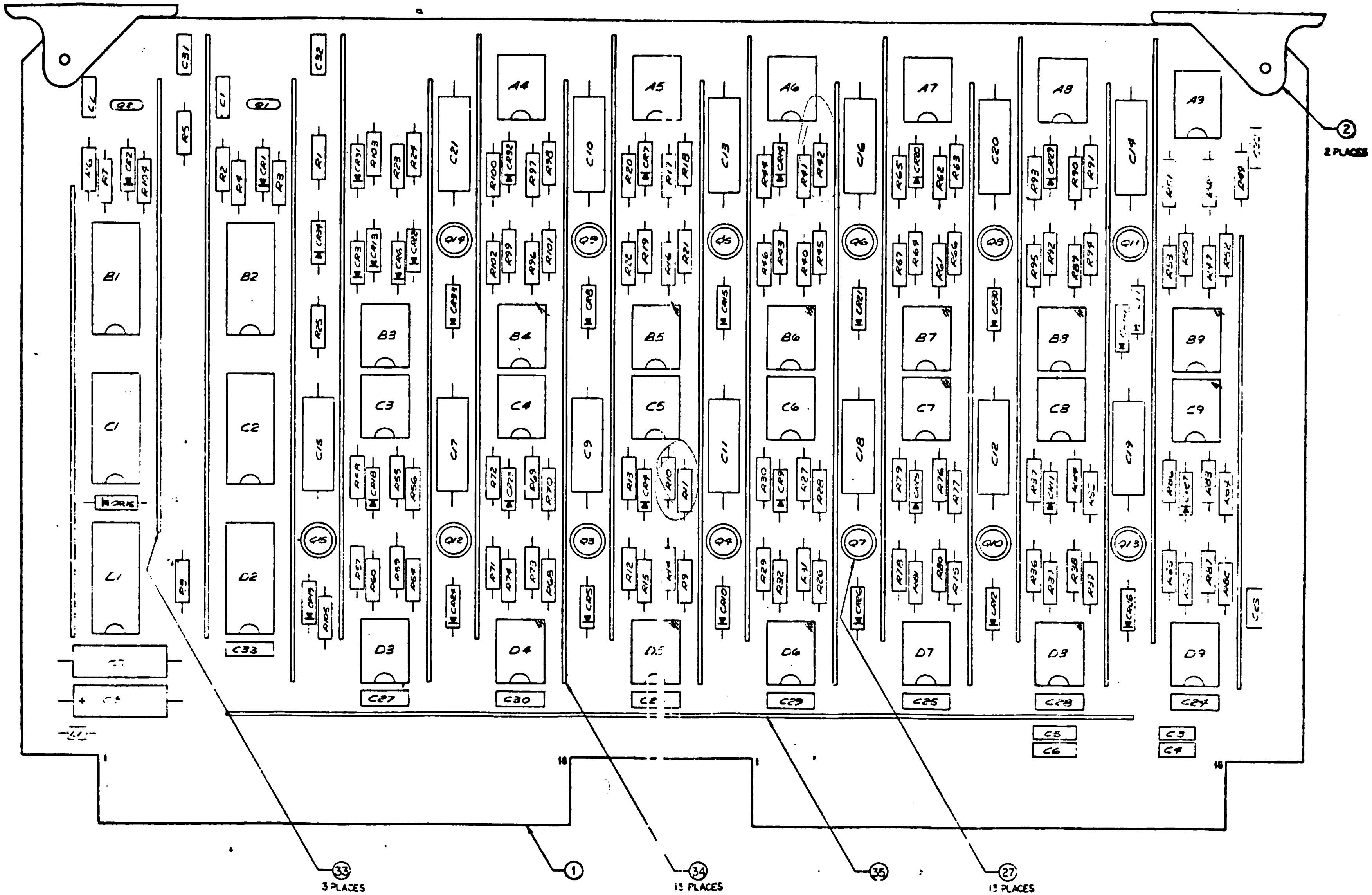
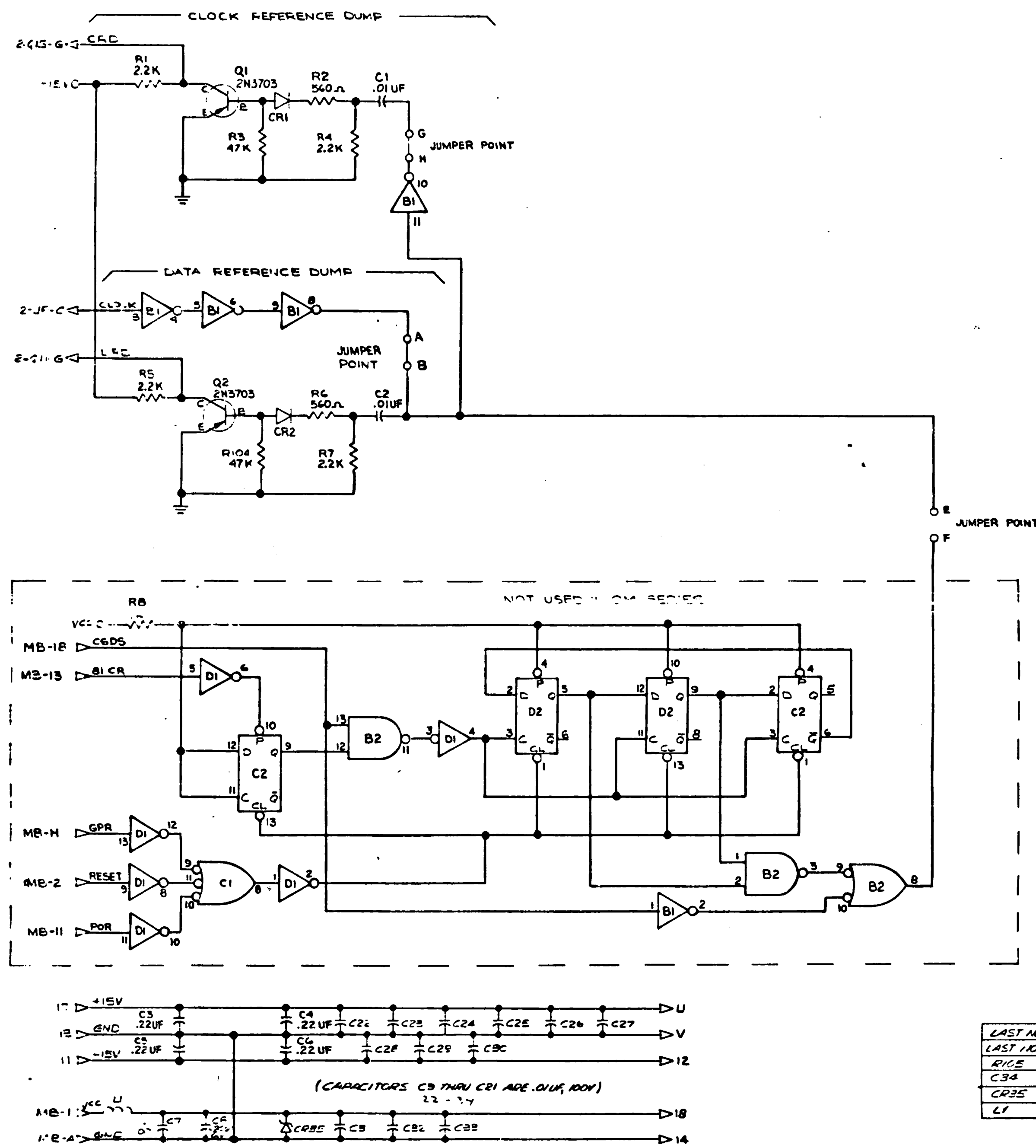


Figure A7. Data Card Assembly - Dwg. No. 1540872 C



LAST NUMBER USED	
LAST I/O	UNUSED
R105	
C34	
CR35	
L1	

Figure A8. Data Card Schematic (Sheet 1 of 2) - Dwg. No. 1540873.C

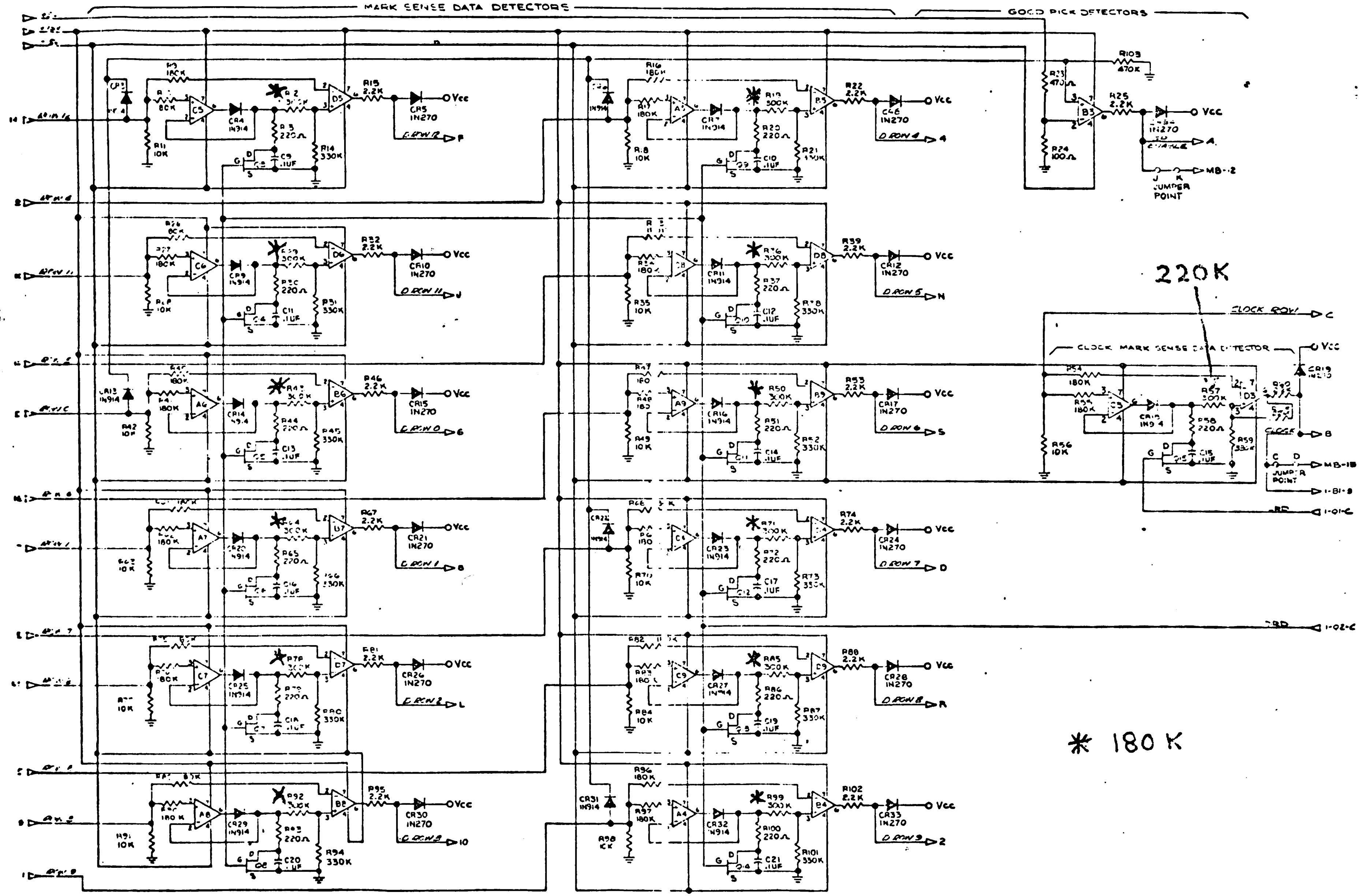


Figure A8. Data Card Schematic (Sheet 2 of 2)

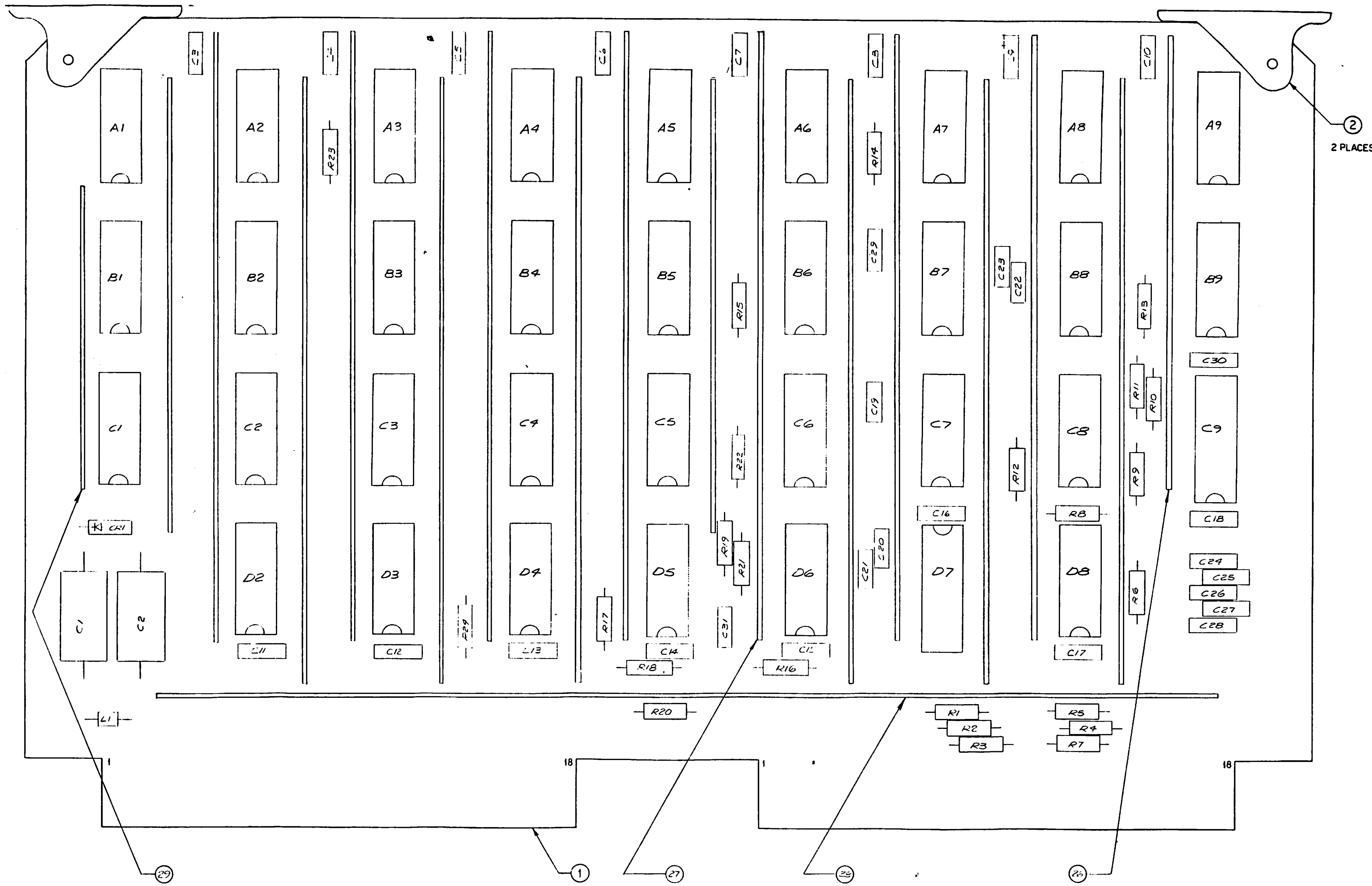


Figure A9. Control Card Assembly – Dwg. No. 1540889

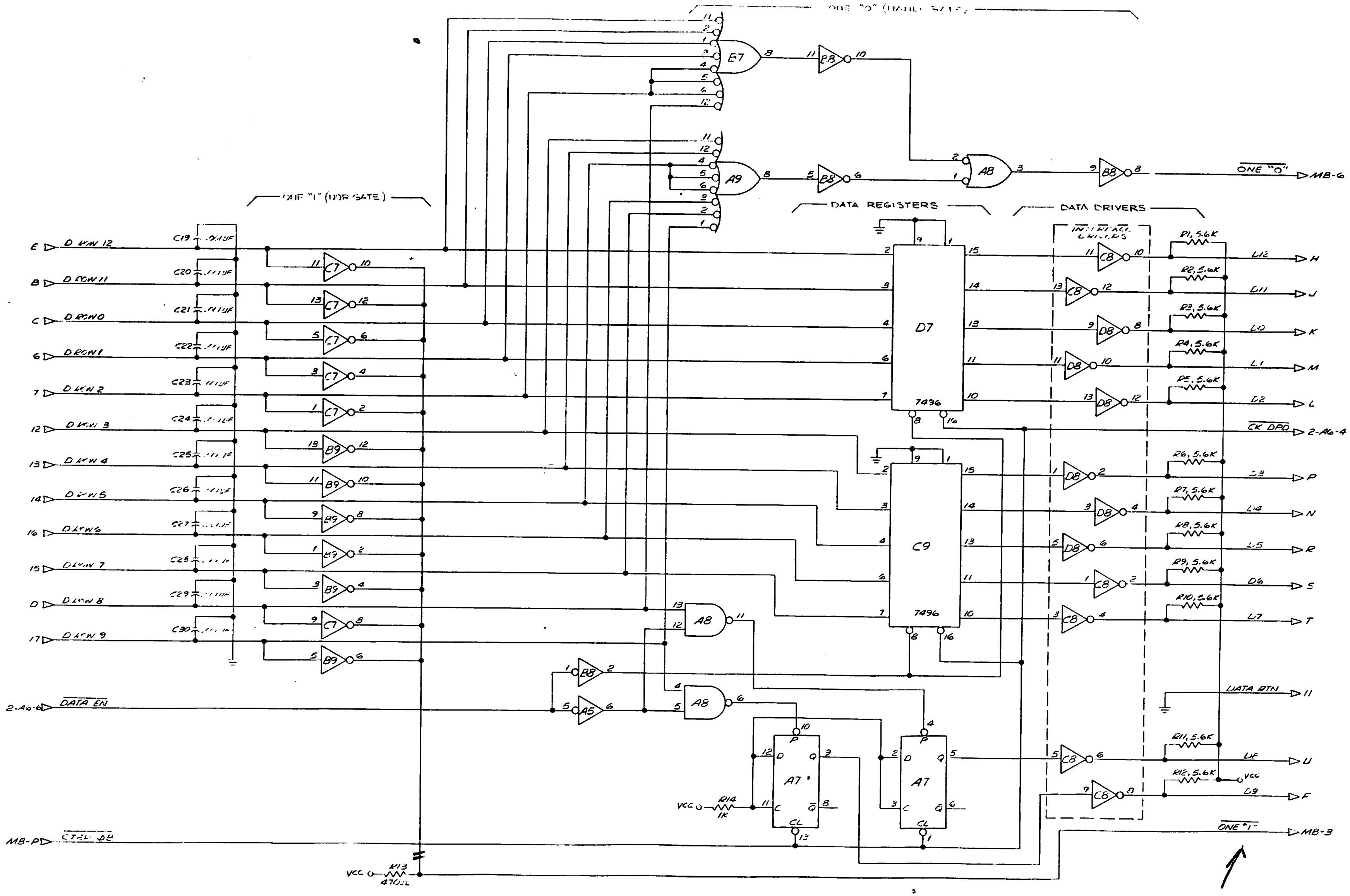


Figure A10. Control Card Schematic (Sheet 1 of3) - Dwg. No. 1540888A

SHOULD BE
HIGH FO 0 CR
81 CR

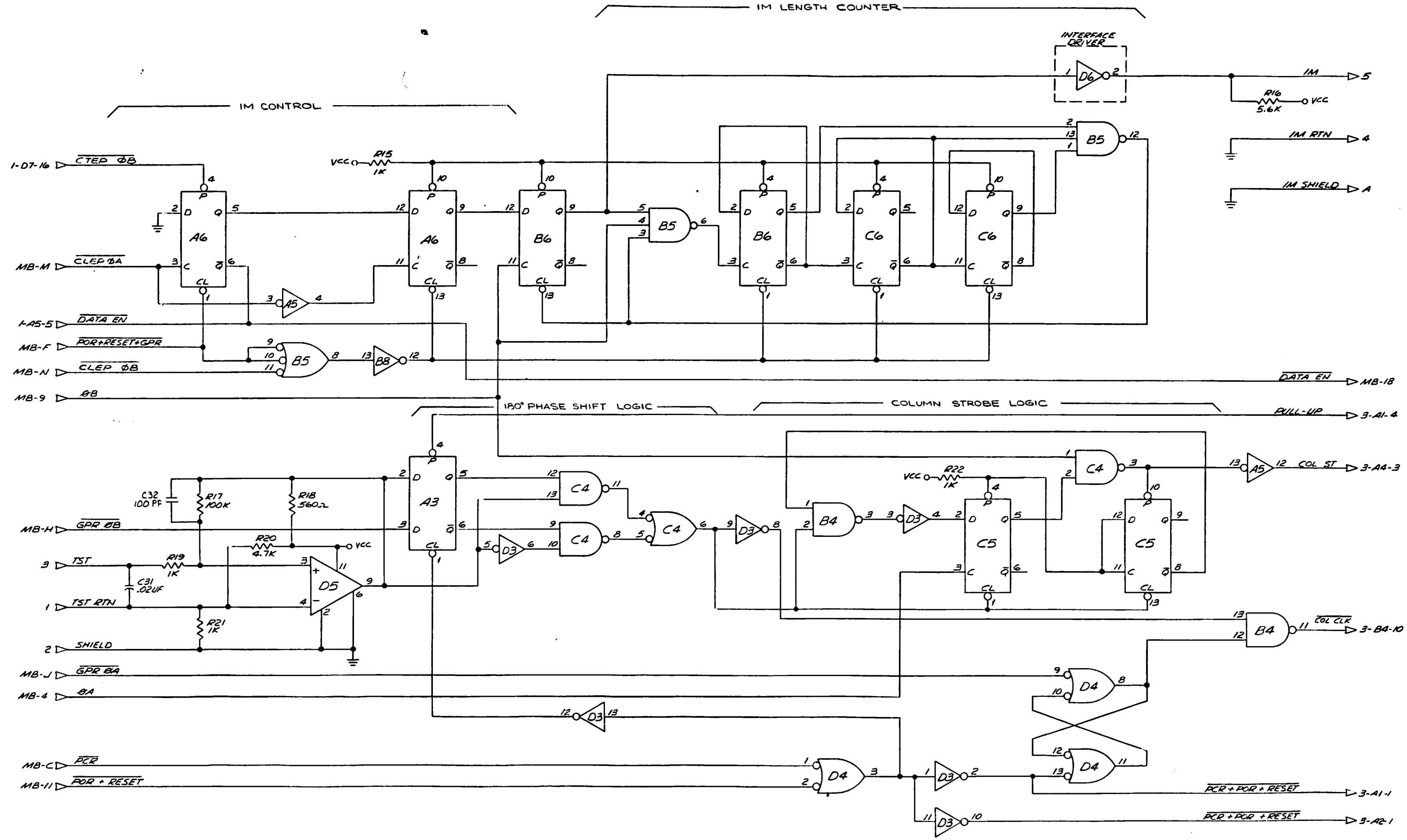


Figure A10. Control Card Schematic (Sheet 2 of 3)

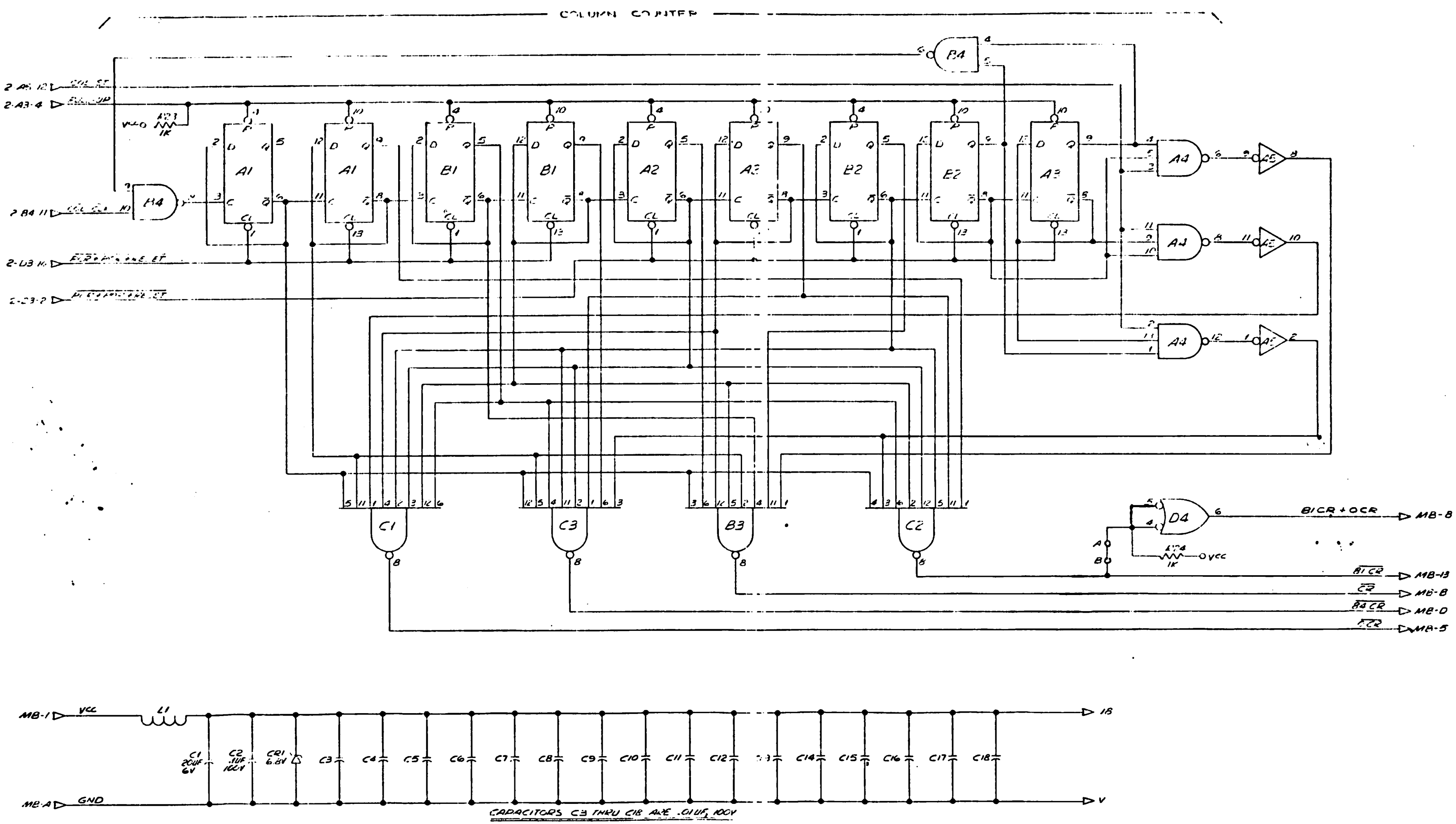


Figure A10. Control Card Schematic (Sheet 3 of 3)

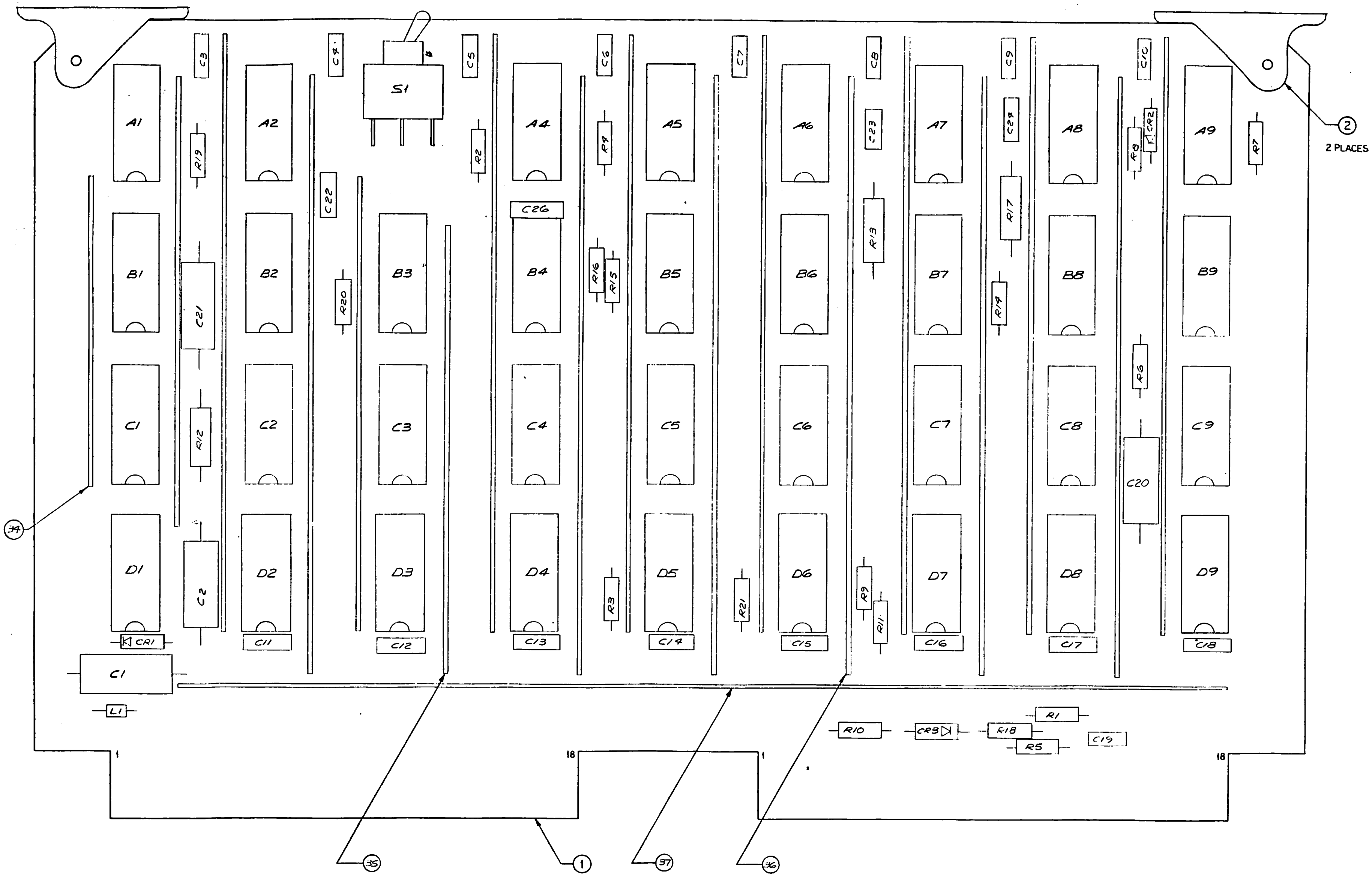


Figure A11. Pick Card Assembly - Dwg. No. 1540881

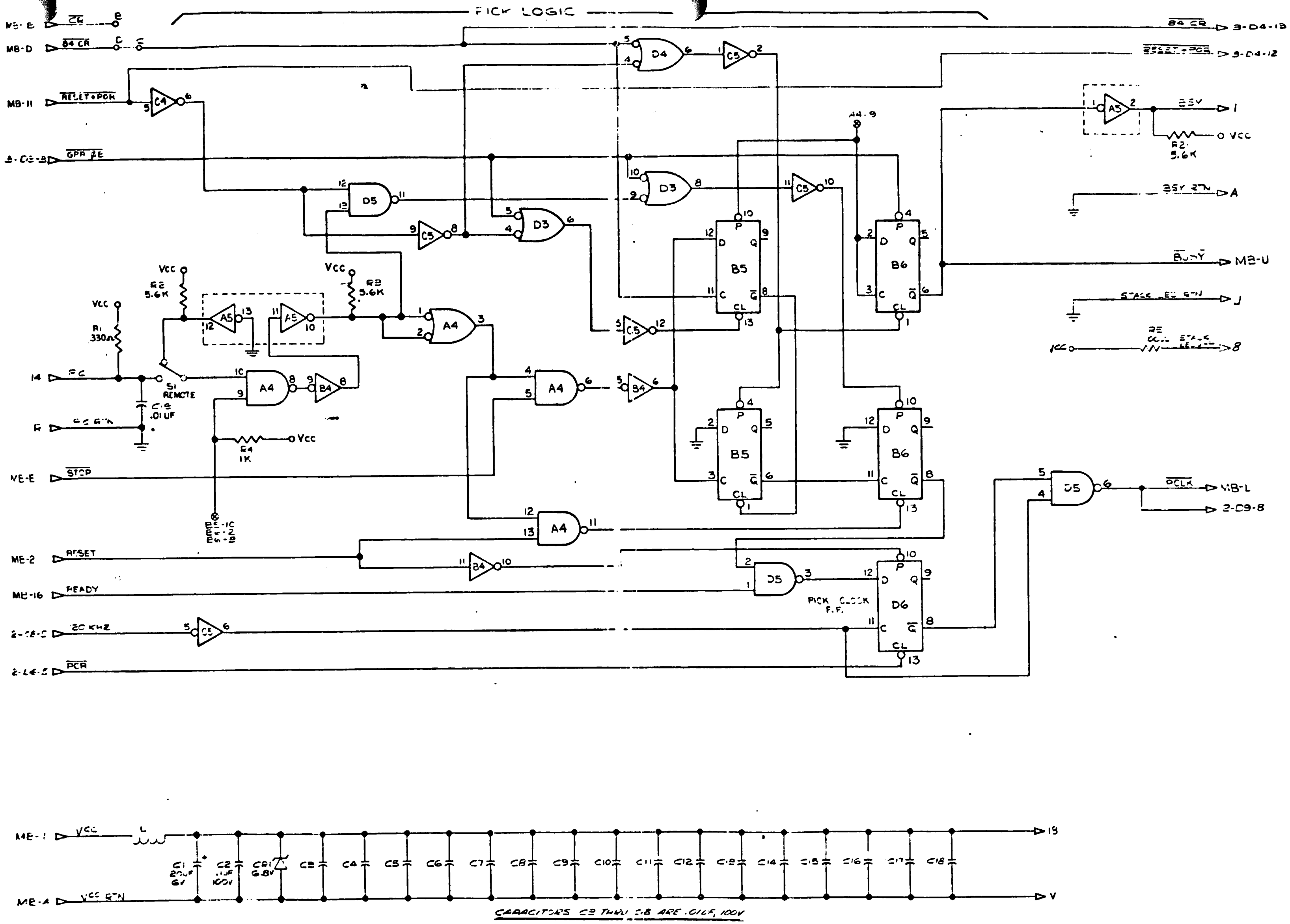


Figure A12. Pick Card Schematic (Sheet 1 of 3)
Dwg. No. 1540882C

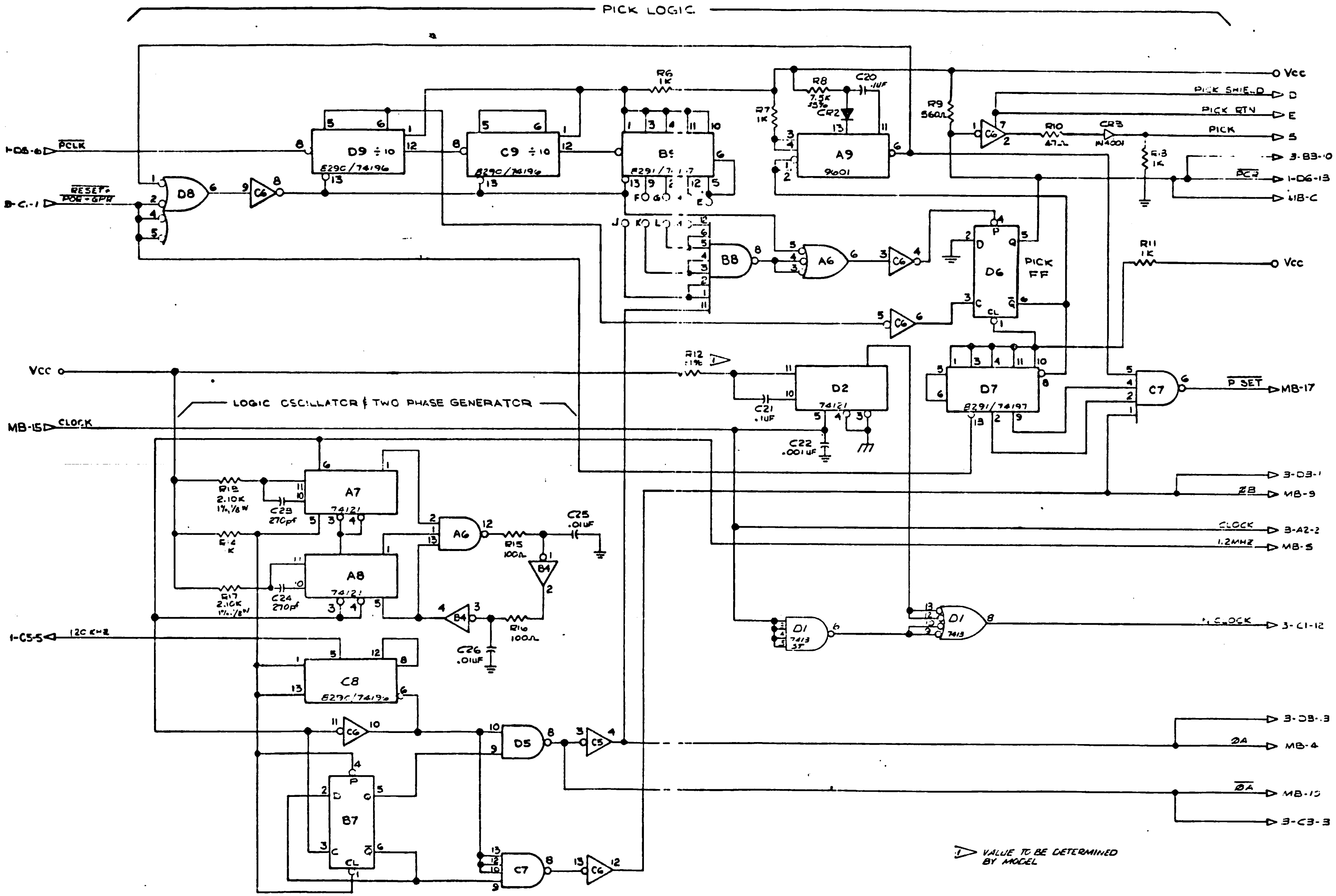


Figure A12. Pick Card Schematic (Sheet 2 of 3)

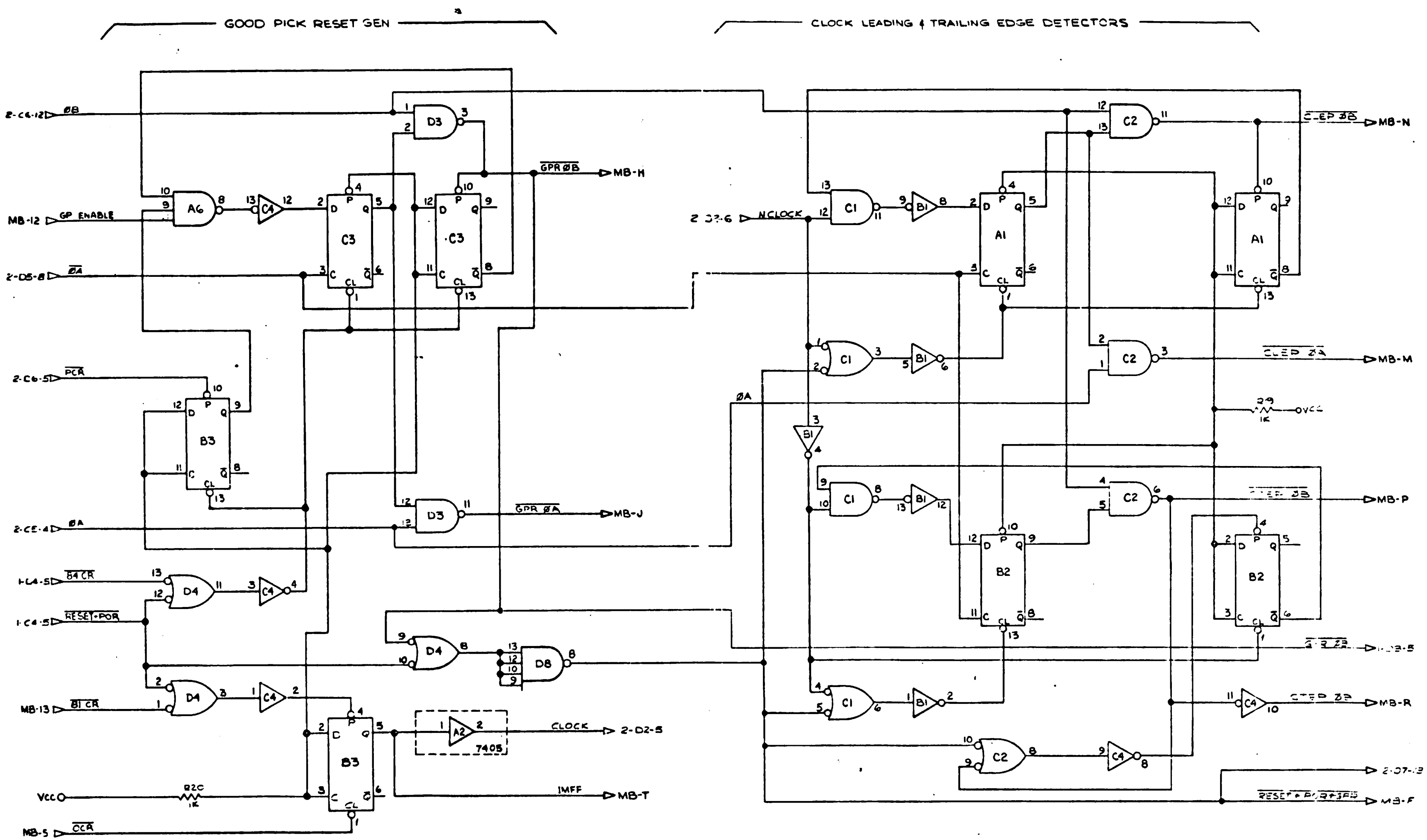


Figure A12. Pick Card Schematic (Sheet 3 of 3)